KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Service Manual

Reference No. : SM- LCT422DAIA1PS-001
Revision : 0
Date : 2006.Nov.
Page : P.1 of 127

In House Model No. : LCT422D
Customer Model No. : LCT42HA36

BOM No : LCT422DAIA1PS–A01

Description : Service Manual for LCT42HA36_LPL _USA

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Mechanical Engineer

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Received By: MK Department

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0	Initial Release	2006-Nov-27

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SERVICE MANUAL

Model: LCT42HA36

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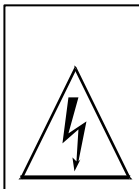
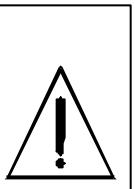
This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

I. Safety Instructions



CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN



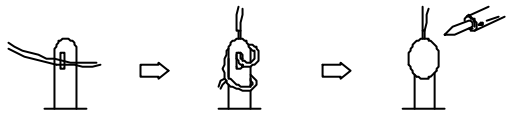
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated " dangerous voltage" within the product' s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

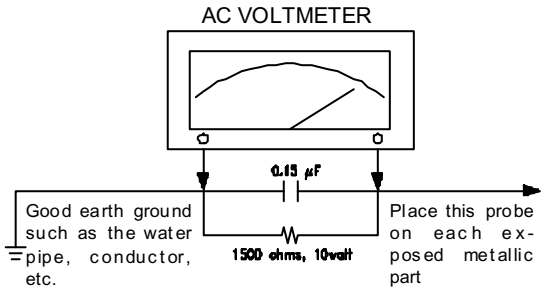
Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.
Please leave them at an appropriate depot.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15µF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time.
   Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.


AC VOLTMETER
0.15 µF
Good earth ground such as the water pipe, conductor, etc.
1500 ohms, 10watt
Place this probe on each exposed metallic part
AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.

1. Do not power on.

1.1 Please check AC cable if connect to AC plug.

Is true the connector don’t connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don’t connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J39,J31 .If not connector direction is wrong.

Or the mainboard somewhere of power short circuit.

3.The power is normal work ,but don’t backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q18collect if not has +5v voltage.

Is true Q18 collect hasn’t +5v ,To check Q18 if fail. Or to check Q18 of base if not low.

(Low is working, high don’t work).

Please refer to attached sheet A circuit diagram.

3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

3.3 To check connector panel of voltage is +24v. It’s true .Then to check of the first pin if it have +5V voltage, It’s true , than to check power board of +24v voltage ,It’s true. The panel of backlight board is fail. The change panel of backlight board.

Please refer to attached sheet B Panel of datasheet.

4.The screen don’t have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of bead L69 and L57 connect if not OK.Then check the L69 and L57 of voltage is +12v(27 inch panel voltage is +5v, To check L68 and L56) . Next to check fuse F1 and connector J10 if not is +12v(27 inch panel voltage is +5v). If isn’t please check power board of connector CON5 if has +12v(27 inch panel voltage is +5v).

4.2To check to main board +12 V voltage. To check to main board IC U35 of the first pin if

+5v voltage ,It’s fail. It’s low (close 0 v) working.

The circuit diagram follow down:

Please refer to attached sheet A circuit diagram.

5.The remote control don’t be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connecter J21 of wire connect fastness and the connecter of wire open.

Please refer to attached sheet A circuit diagram.

6.The sound don’t output.

7.1 To check main board +24v voltage of connector J8 ,It’s true not +24v voltage. Then to to check power main +24v fail .

Please refer to attached sheet A circuit diagram.

7.The DTV don’t detect .

7.1 To check mainboard of connecter J24 and DTV mainboard of connector HA1 of FCC wire if no connect fastness.

Please refer to attached sheet C of DTV circuit diagram.

Production Specification

Product Model:	LCT42HA36
Screen Size:	42” diagonal
Screen Area:	930.25mm(H) x 523.01mm(V)
Aspect Ratio:	16:9
External Size:	1067.3mm(W) x 781.2mm(H) x 275.0mm(D) (with Stand)
Gross Weight:	34 kg
Resolution:	1366 (H) x 768 (V) pixels (Each pixel has R/G/B 3 color cells)
Color:	16.7 millions of colors (R/G/B each 256 scales)
Gray Scale:	256 (R/G/B each 8-bit)
Peak Brightness:	500cd/m^2
Contrast (Dark Room):	800:1 (Typical)
TV System:	NTSC M, ATSC
Sound:	Mono, Stereo, SAP (BTSC)
Sound Effect:	Acoustic Cinema Enhancement
Power Supply:	AC 120V, 60Hz
Power Consumption:	300W
Input/Output Terminal:	Antenna Input (F Type) x 2 (NTSC & ATSC)
	RS-232 (D-Sub 9 Pin Type) x 1 (Only for DTV)
	VGA (D-Sub 15 Pin Type) x 1
	HDMI (Ver 1.1) connector x 1
	Component Video - YPbPr x 2 (RCA Terminals)
	Video Input (RCA Terminals) x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
	1 set of Audio Output terminals (RCA, L&R)
	SPDIF (Optical) x 1 (Only for ATSC)
Agent System:	UL, cUL, FCC

NOTE:

- *The specifications shown above may be changed without notice for quality improvement.*

Support the Signal Mode

A. D-Sub Mode (VGA)

Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
	37.86	72.81
800 x 600	35.16	56.25
	37.90	60.32
	48.08	72.19
1024 x 768	48.40	60.00

B. HDTV Mode (YPbPr)

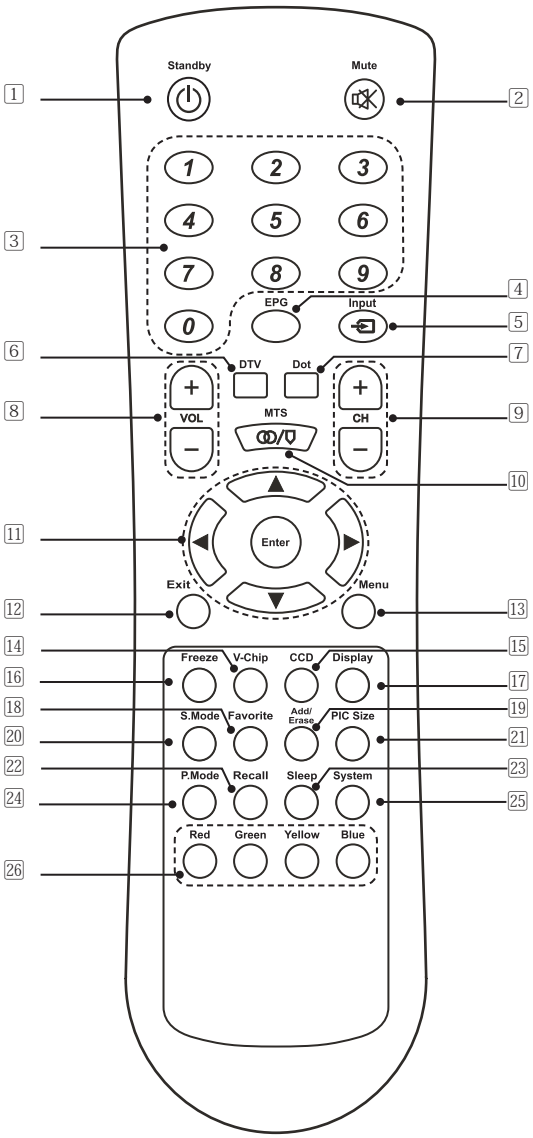
Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00

C. HDMI Mode

Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00

- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

Remote Control



1. **Power** (⏻): Press to turn on and off.
2. **Mute** (🔇): Press to mute the sound. Press again or press **VOL**+/- to restore the sound.
3. **0~9 Number Buttons**: In TV mode, press 0~9 to select a channel; the channel changes after 2 seconds.
4. **EPG**: Press to display EPG (Electronic Program Guide) menu.
5. **Input** (⏏): Press to select the signal sources.
6. **DTV**: Press to select Digital TV mode.
7. **Dot**: Press number buttons with it to select the channels directly in DTV.
8. **VOL +/-**: Press to adjust the volume.
9. **CH +/-**: Press to changes channels.
10. **MTS**: Press to repeatedly to cycle through the Multi-channel TV sound (MTS) options. Such as Stereo, Mono, or Separate Audio Program (SAP broadcast).
11. ◀,▲,▼,▶, **Enter**: Press ◀,▲,▼,▶ to move the on-screen cursor. To select an item, press **Enter** to confirm.
12. **Exit**: Press to return or exit the OSD menu.
13. **Menu**: Press to display the OSD menu.
14. **V-Chip**: Press to se lect the child protect mode.
15. **CCD**: Press to select the Closed Caption mode.
16. **Freeze**: Press to freeze the picture, press again to restore the picture. (This button is not avaiable for VGA mode.)
17. **Display**: Press to display the channel information and it disappear after 3 seconds.
18. **Favorite**: Press repeatedly to cycle through the favorite channel list.
19. **Add/Erase**: Press to add or delete favorite channel.
20. **S.Mode**: Adjust the TV sound by selecting one of the preset factory settings, such as Normal, News, Cinema, Concert, or User.
21. **PIC.Size**: Press to change the screen size, such as Full, 4:3, Panoramic. (Note: In VGA mode, it can select picture size is Full. While in DTV mode, it can select picture size is: Full and 4:3.)
22. **Recall**: Press to return to previous channel.
23. **Sleep**: Press to sleep a time for theTV to turn off automatically, such as 15Min, 30Min, 60Min, 90Min, 120Min and, OFF. To cancel sleep time, press Sleep repeatedly until sleep OFF appears.
24. **P.Mode**: Adjust the TV picture by selecting one of the preset factory settings, such as Hi-Bright, User, Cinema, Normal and Vivid.
25. **System**: Press repeatedly to cycle through the system options: AUTO, NTSC3.58 and PAL.(This button is activate for AV, S-Video input source.)
26. **Color Buttons**:
    Red: Press this button to access the red item or page.
    Blue: Press this button to access the blue item or page.
    Green: Press this button to access the green item or page.
    Yellow: Press this button to access the yellow item or page.

Optical Output

Flash 32mb

MT5351 MPEG Decoder

DDR 256M

DDR 256M

TD1336 Digital Tuner

X6965D SAW Filter

MT5111 DTV Demodulator

DTV BOARD

POWER BOARD

5V

Standby 5V

12V

9V

24VA (For Class D)

24V (For LCD Panel)

MAIN BOARD

HDMI

MT8293 HDMI Receiver

74L VC245A X4 24 bit RGB Switch

Analog Tuner

To panel

YPbPr1

YPbPr2 (Option)

QS3VH257 Switch(Option)

MT8202 ADC & Scaler & LVDS Transfer

Flash 8M/16M

VGA

NJRC4558 Audio Buffer

Audio Output

AV

DDR 128M

S-Video

DDR 128M

Audio X2

HEF4052 Switch

WM8776 Audio ADC&DAC

Max232 Level Shift

RS232 Socket

Audio X3

R2S15102 Class D Amplifier

Relay

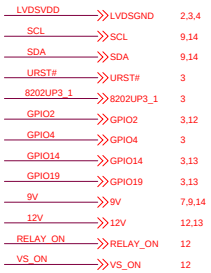
Speaker

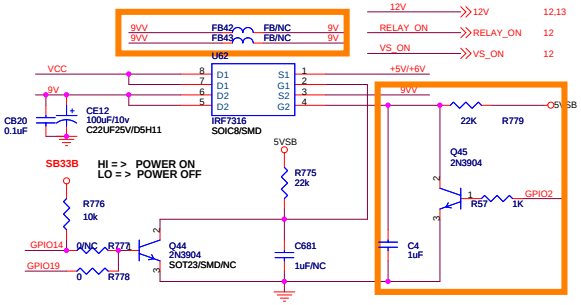
LCD panel

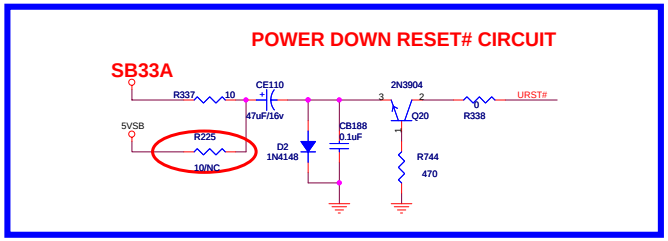
MT8202E (PBGA388) LCDTV BOARD 4 LAYERS FOR AKAI

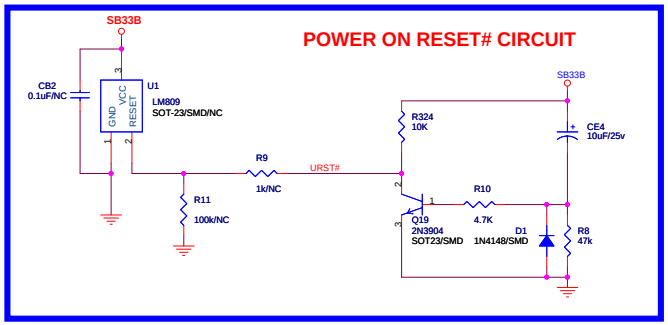
1. INDEX / POWER / RESET / EEPROM
2. LDO
3. MT8202E PBGA388
4. MT8202 DECOUPLING
5. DDR MEMORY & FLASH
6. MT5351 INTERFACE
7. HDMI MT8293
8. DAUGHTER BOARD IN
9. WM8776 & VIDEO BYPASS
10. AUDIO / VIDEO IN CIRCUIT
11 . VGA & PC AUDIO IN
12. LVDS OUT
13. BACK LIGHT / KEYPAD
14. TUNER IN
15. AV IN
16. AUDIO IN
17.AUDIO Amplifier

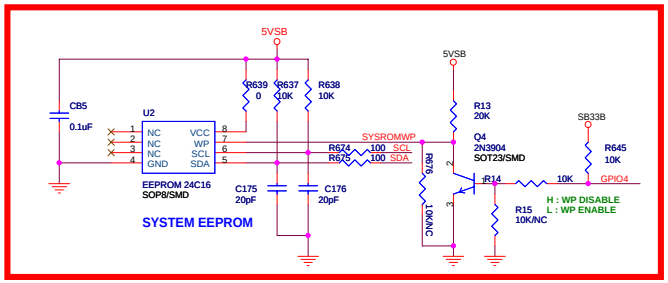
Rev	History	P#	Date
AKAI_MT8202_27US_LVDS_V0.0	New		2005/11/22
AKAI_MT8202_27US_HDMI_LVDS_V0.0	ADD HDMI / VIDEO /AUDIO CONNECTOR INPUT IN		

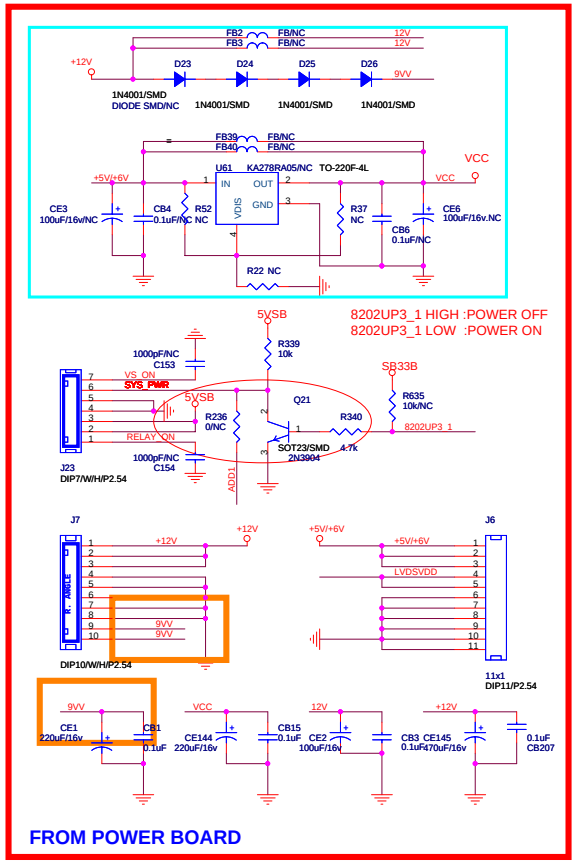


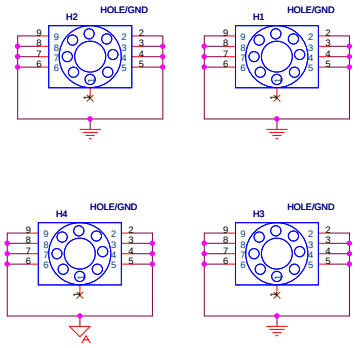












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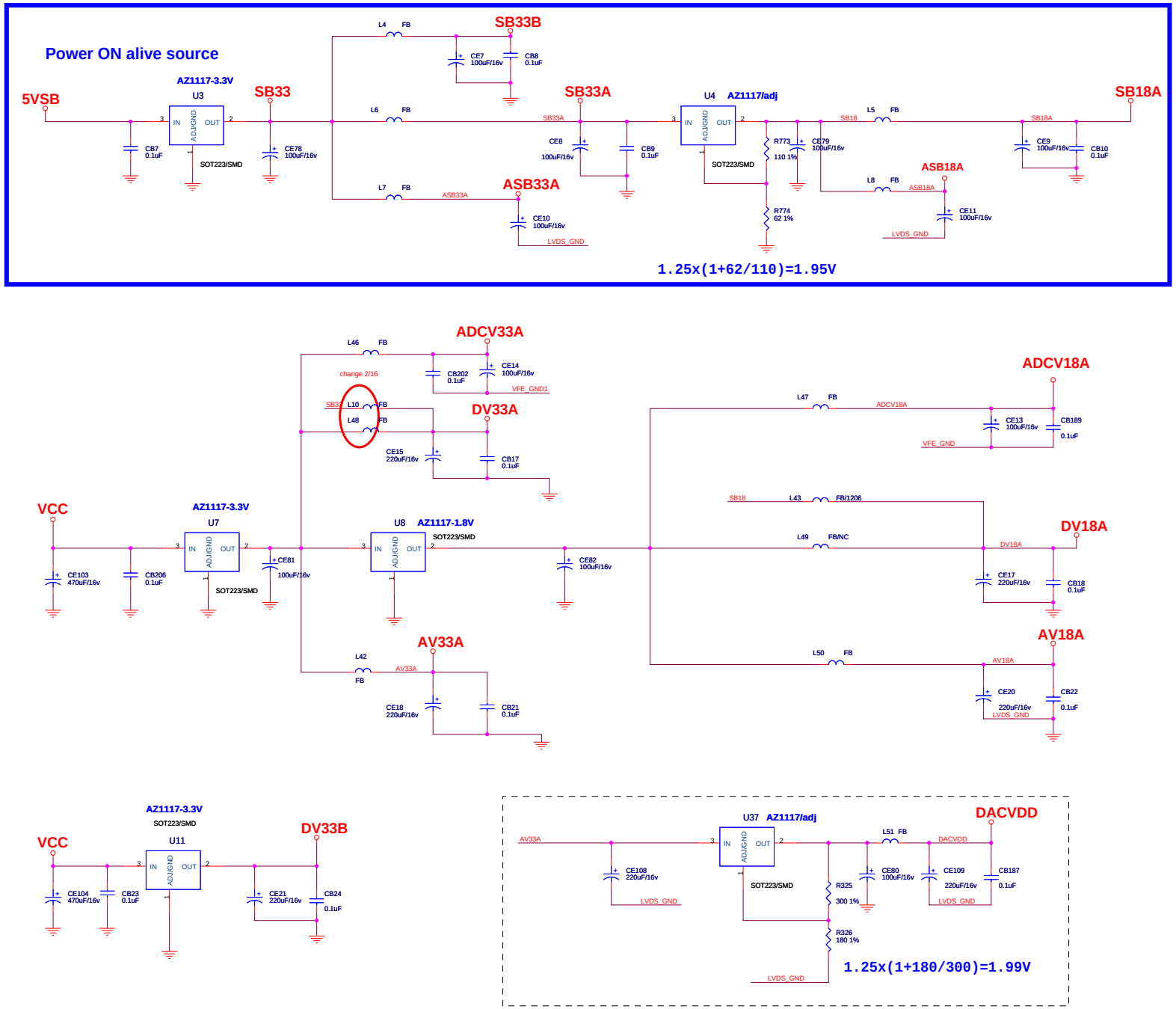
Date: Thursday, April 13, 2006		Sheet 1	17



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		Checked: <Checker>	
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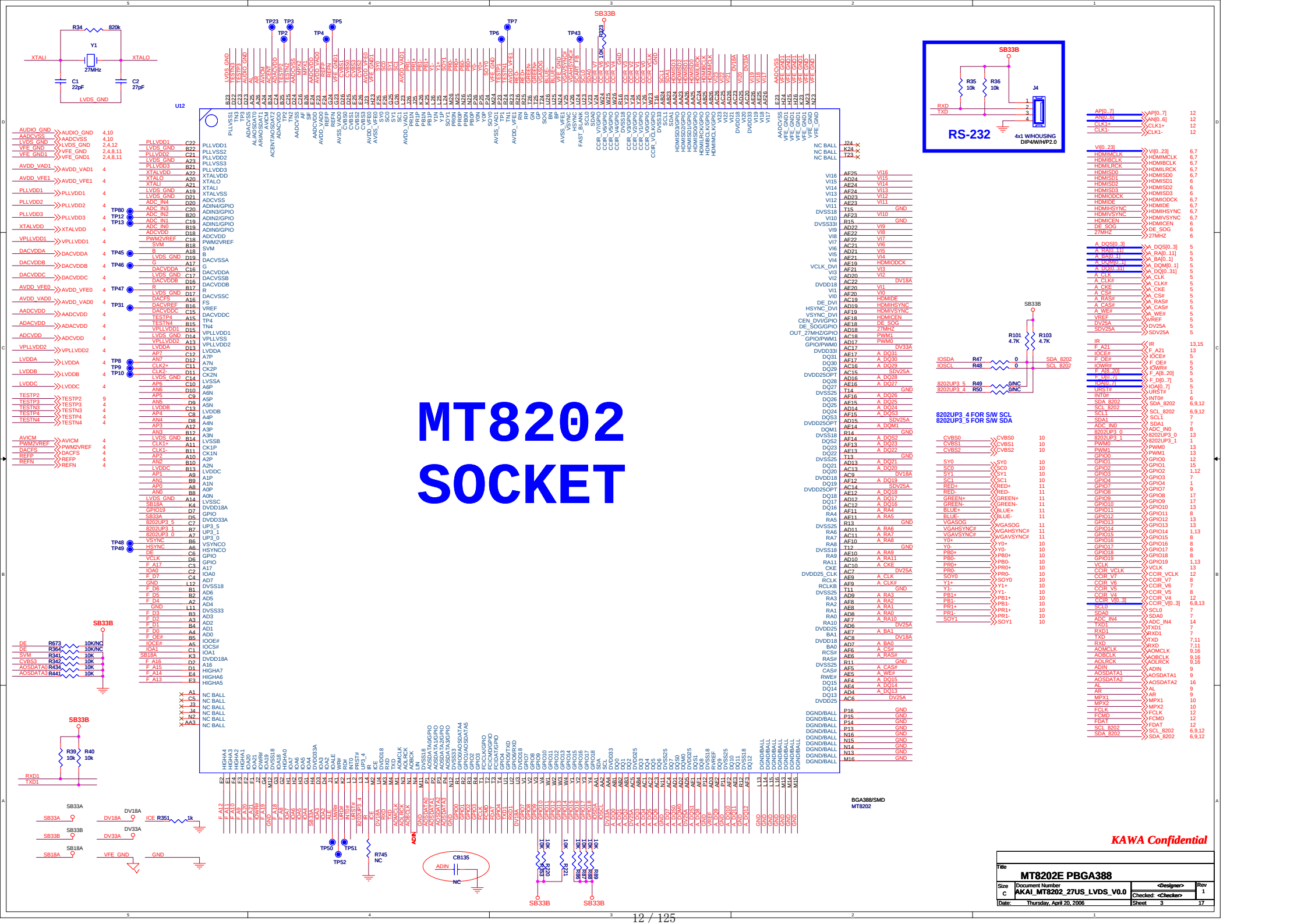
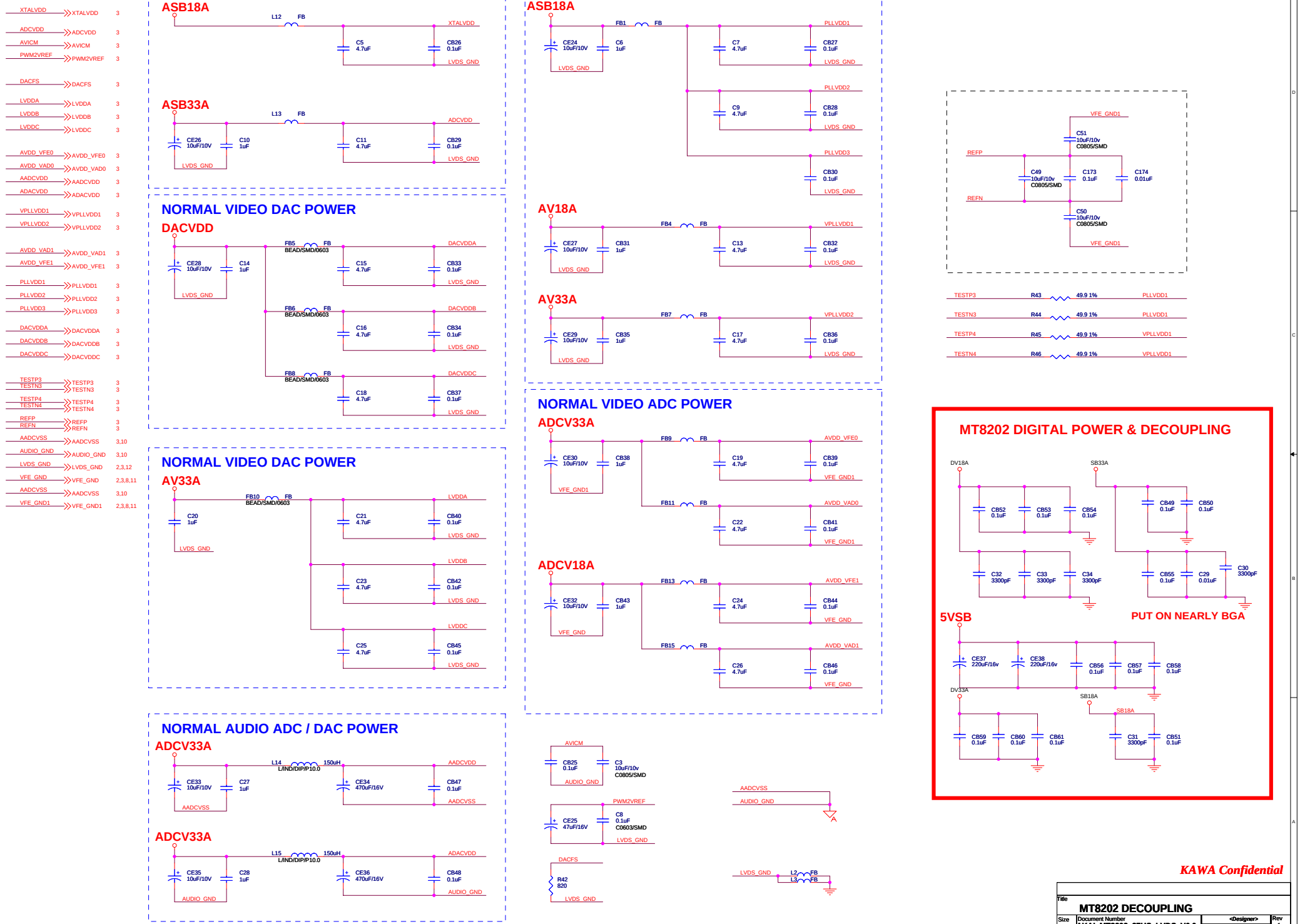

MT8202
SOCKET
U12
SB33B
RS-232
4x1 W/HOUSING
DIP4/W/H/P2.0
8202UP3_4 FOR S/W SCL
8202UP3_5 FOR S/W SDA
BGA388/SMD
MT8202
KAWA Confidential
MT8202E PBGA388
AKAI_MT8202_27US_LVDS_V0.0
Thursday, April 20, 2006


XTALVDD 3
ADCVDD 3
AVICM 3
PWM2VREF 3
DACFS 3
LVDDA 3
LVDDB 3
LVDDC 3
AVDD_VFE0 3
AVDD_VAD0 3
AADCVDD 3
ADACVDD 3
VPLLVDD1 3
VPLLVDD2 3
AVDD_VAD1 3
AVDD_VFE1 3
PLLVDD1 3
PLLVDD2 3
PLLVDD3 3
DACVDDA 3
DACVDDB 3
DACVDDC 3
TESTP3 3
TESTN3 3
TESTP4 3
TESTN4 3
REFP 3
REFN 3
AADCVSS 3,10
AUDIO_GND 3,10
LVDS_GND 2,3,12
VFE_GND 2,3,8,11
AADCVSS 3,10
VFE_GND1 2,3,8,11
STANDBY ANALOG POWER
ASB18A
L12 FB
C5 4.7uF
CB26 0.1uF
XTALVDD
LVDS_GND
ASB33A
L13 FB
CE26 10uF/10V
C10 1uF
C11 4.7uF
CB29 0.1uF
ADCVDD
LVDS_GND
NORMAL VIDEO DAC POWER
DACVDD
CE28 10uF/10V
C14 1uF
FB5 FB BEAD/SMD/0603
C15 4.7uF
CB33 0.1uF
DACVDDA
FB6 FB BEAD/SMD/0603
C16 4.7uF
CB34 0.1uF
DACVDDB
FB8 FB BEAD/SMD/0603
C18 4.7uF
CB37 0.1uF
DACVDDC
NORMAL VIDEO DAC POWER
AV33A
C20 1uF
FB10 FB BEAD/SMD/0603
C21 4.7uF
CB40 0.1uF
LVDDA
C23 4.7uF
CB42 0.1uF
LVDDB
C25 4.7uF
CB45 0.1uF
LVDDC
NORMAL AUDIO ADC / DAC POWER
ADCV33A
L14 150uH L/IND/DIP/P10.0
CE33 10uF/10V
C27 1uF
CE34 470uF/16V
CB47 0.1uF
AADCVDD
AADCVSS
ADCV33A
L15 150uH L/IND/DIP/P10.0
CE35 10uF/10V
C28 1uF
CE36 470uF/16V
CB48 0.1uF
ADACVDD
AUDIO_GND
NORMAL ANALOG POWER
ASB18A
FB1 FB
CE24 10uF/10V
C6 1uF
C7 4.7uF
CB27 0.1uF
PLLVDD1
C9 4.7uF
CB28 0.1uF
PLLVDD2
CB30 0.1uF
PLLVDD3
AV18A
FB4 FB
CE27 10uF/10V
CB31 1uF
C13 4.7uF
CB32 0.1uF
VPLLVDD1
AV33A
FB7 FB
CE29 10uF/10V
CB35 1uF
C17 4.7uF
CB36 0.1uF
VPLLVDD2
NORMAL VIDEO ADC POWER
ADCV33A
CE30 10uF/10V
CB38 1uF
FB9 FB
C19 4.7uF
CB39 0.1uF
AVDD_VFE0
VFE_GND1
FB11 FB
C22 4.7uF
CB41 0.1uF
AVDD_VAD0
ADCV18A
CE32 10uF/10V
CB43 1uF
FB13 FB
C24 4.7uF
CB44 0.1uF
AVDD_VFE1
VFE_GND
FB15 FB
C26 4.7uF
CB46 0.1uF
AVDD_VAD1
AVICM
CB25 0.1uF
C3 10uF/10v C0805/SMD
PWM2VREF
CE25 47uF/16V
C8 0.1uF C0603/SMD
DACFS
R42 820
AADCVSS
AUDIO_GND
LVDS_GND
L2 FB
L3 FB
VFE_GND1
C51 10uF/10v C0805/SMD
REFP
C49 10uF/10v C0805/SMD
C173 0.1uF
C174 0.01uF
REFN
C50 10uF/10v C0805/SMD
TESTP3 R43 49.9 1% PLLVDD1
TESTN3 R44 49.9 1% PLLVDD1
TESTP4 R45 49.9 1% VPLLVDD1
TESTN4 R46 49.9 1% VPLLVDD1
MT8202 DIGITAL POWER & DECOUPLING
DV18A
SB33A
CB52 0.1uF
CB53 0.1uF
CB54 0.1uF
CB49 0.1uF
CB50 0.1uF
C32 3300pF
C33 3300pF
C34 3300pF
CB55 0.1uF
C29 0.01uF
C30 3300pF
PUT ON NEARLY BGA
5VSB
CE37 220uF/16v
CE38 220uF/16v
CB56 0.1uF
CB57 0.1uF
CB58 0.1uF
DV33A
SB18A
CB59 0.1uF
CB60 0.1uF
CB61 0.1uF
C31 3300pF
CB51 0.1uF
KAWA Confidential
Title
MT8202 DECOUPLING
Size C
Document Number AKAI_MT8202_27US_LVDS_V0.0
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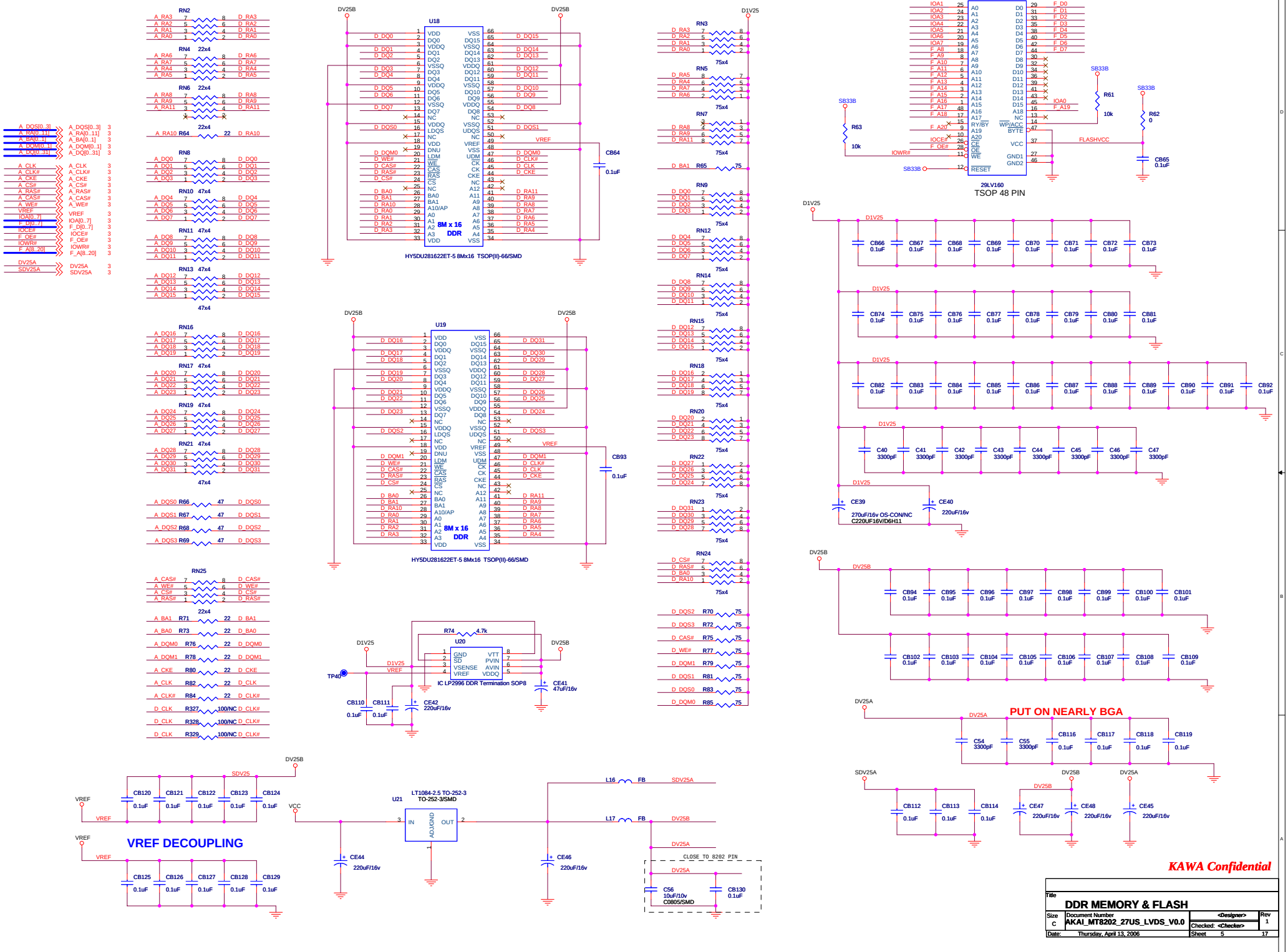
RN2
RN4 22x4
RN6 22x4
RN8
RN10 47x4
RN11 47x4
RN13 47x4
RN16
RN17 47x4
RN19 47x4
RN21 47x4
RN25
R64 22
R66 47
R67 47
R68 47
R69 47
R71 22
R73 22
R76 22
R78 22
R80 22
R82 22
R84 22
R327 100/NC
R328 100/NC
R329 100/NC
U18
HY5DU281622ET-5 8Mx16 TSOP(II)-66/SMD
U19
HY5DU281622ET-5 8Mx16 TSOP(II)-66/SMD
8M x 16 DDR
RN3
RN5
RN7
RN9
RN12
RN14
RN15
RN18
RN20
RN22
RN23
RN24
R65 75
R70 75
R72 75
R75 75
R77 75
R79 75
R81 75
R83 75
R85 75
U17
29LV160
TSOP 48 PIN
R61 10k
R62 0
R63 10k
CB64 0.1uF
CB65 0.1uF
CB66 0.1uF
CB67 0.1uF
CB68 0.1uF
CB69 0.1uF
CB70 0.1uF
CB71 0.1uF
CB72 0.1uF
CB73 0.1uF
CB74 0.1uF
CB75 0.1uF
CB76 0.1uF
CB77 0.1uF
CB78 0.1uF
CB79 0.1uF
CB80 0.1uF
CB81 0.1uF
CB82 0.1uF
CB83 0.1uF
CB84 0.1uF
CB85 0.1uF
CB86 0.1uF
CB87 0.1uF
CB88 0.1uF
CB89 0.1uF
CB90 0.1uF
CB91 0.1uF
CB92 0.1uF
C40 3300pF
C41 3300pF
C42 3300pF
C43 3300pF
C44 3300pF
C45 3300pF
C46 3300pF
C47 3300pF
CE39 270uF/16v OS-CON/NC C220UF16V/D6H11
CE40 220uF/16v
CB93 0.1uF
CB94 0.1uF
CB95 0.1uF
CB96 0.1uF
CB97 0.1uF
CB98 0.1uF
CB99 0.1uF
CB100 0.1uF
CB101 0.1uF
CB102 0.1uF
CB103 0.1uF
CB104 0.1uF
CB105 0.1uF
CB106 0.1uF
CB107 0.1uF
CB108 0.1uF
CB109 0.1uF
PUT ON NEARLY BGA
C54 3300pF
C55 3300pF
CB116 0.1uF
CB117 0.1uF
CB118 0.1uF
CB119 0.1uF
CB112 0.1uF
CB113 0.1uF
CB114 0.1uF
CE47 220uF/16v
CE48 220uF/16v
CE45 220uF/16v
R74 4.7k
U20
IC LP2996 DDR Termination SOP8
TP40
CB110 0.1uF
CB111 0.1uF
CE42 220uF/16v
CE41 47uF/16v
VREF DECOUPLING
CB120 0.1uF
CB121 0.1uF
CB122 0.1uF
CB123 0.1uF
CB124 0.1uF
CB125 0.1uF
CB126 0.1uF
CB127 0.1uF
CB128 0.1uF
CB129 0.1uF
U21
LT1084-2.5 TO-252-3
TO-252-3/SMD
CE44 220uF/16v
CE46 220uF/16v
L16 FB
L17 FB
CLOSE TO 8202 PIN
C56 10uF/10v C0805/SMD
CB130 0.1uF
KAWA Confidential
DDR MEMORY & FLASH
AKAI_MT8202_27US_LVDS_V0.0
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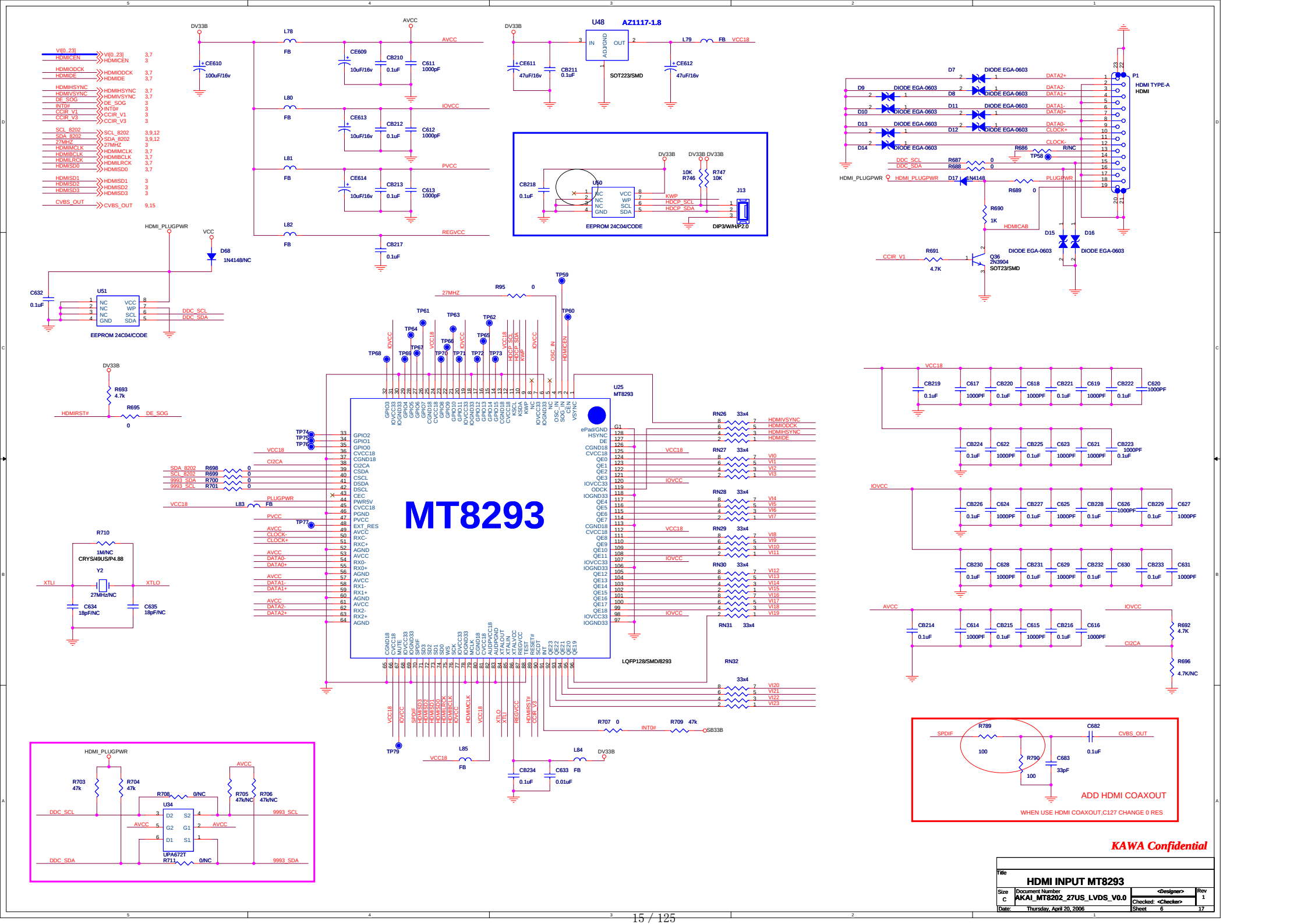
MT8293
U25
MT8293
LQFP128/SMD/8293
U48
AZ1117-1.8
SOT223/SMD
U50
EEPROM 24C04/CODE
DIP3/W/HP2.0
U51
EEPROM 24C04/CODE
U34
UPA672T
P1
HDMI TYPE-A
HDMI
Q36
2N3904
SOT23/SMD
ADD HDMI COAXOUT
WHEN USE HDMI COAXOUT,C127 CHANGE 0 RES
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HDMI INPUT MT8293
Document Number
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1
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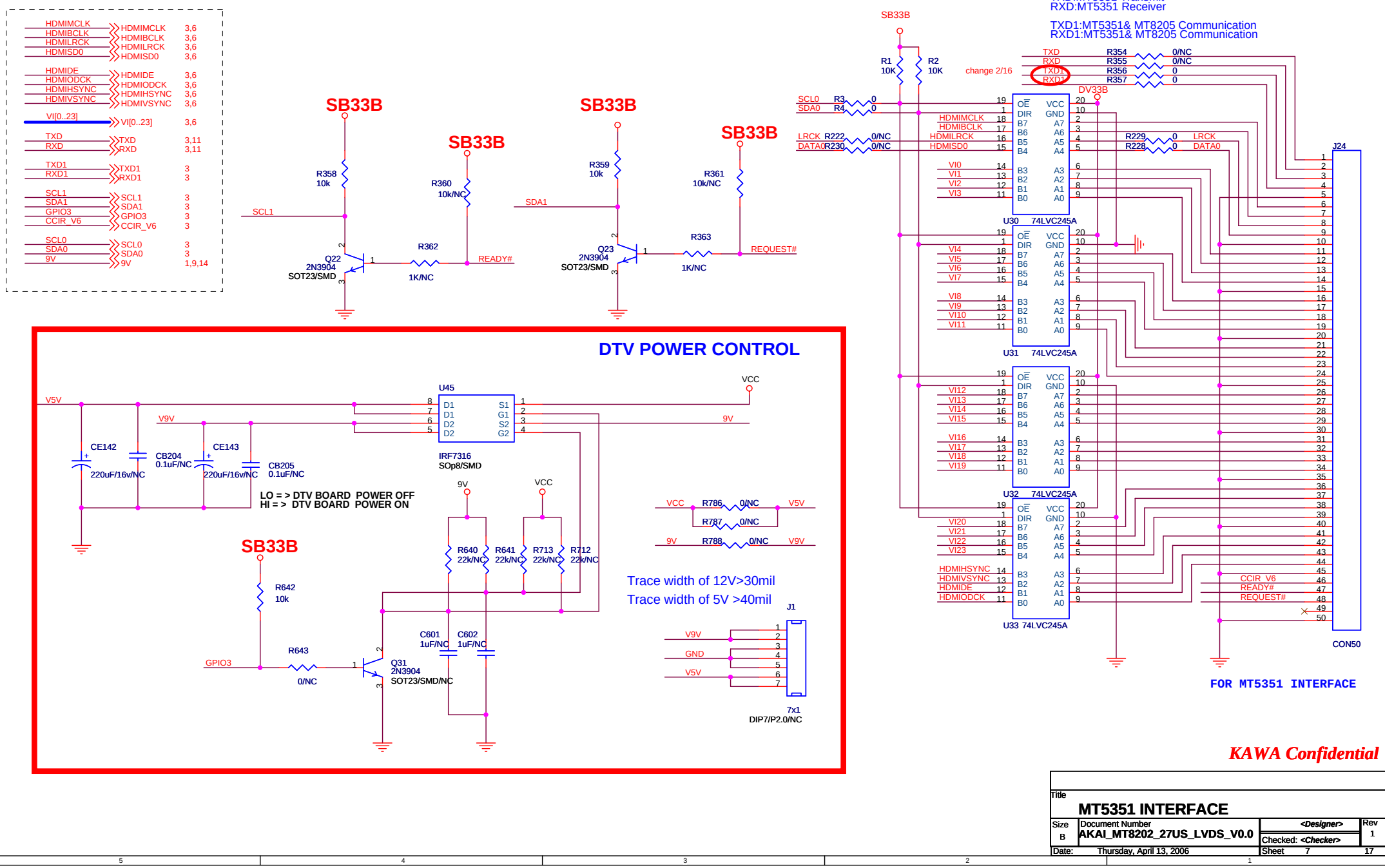
HDMIMCLK 3,6
HDMIBCLK 3,6
HDMILRCK 3,6
HDMISD0 3,6
HDMIDE 3,6
HDMIODCK 3,6
HDMIHSYNC 3,6
HDMIVSYNC 3,6
VI[0..23] 3,6
TXD 3,11
RXD 3,11
TXD1 3
RXD1 3
SCL1 3
SDA1 3
GPIO3 3
CCIR_V6 3
SCL0 3
SDA0 3
9V 1,9,14
SB33B
R358 10k
R360 10k/NC
SCL1
Q22 2N3904 SOT23/SMD
R362
1K/NC
READY#
R359 10k
SDA1
Q23 2N3904 SOT23/SMD
R363
1K/NC
R361 10k/NC
REQUEST#
DTV POWER CONTROL
V5V
V9V
U45
IRF7316 SOp8/SMD
CE142 220uF/16v/NC
CB204 0.1uF/NC
CE143 220uF/16v/NC
CB205 0.1uF/NC
LO = > DTV BOARD POWER OFF
HI = > DTV BOARD POWER ON
VCC
9V
R640 22k/NC
R641 22k/NC
R713 22k/NC
R712 22k/NC
R786 0/NC
R787 0/NC
R788 0/NC
R642 10k
R643 0/NC
GPIO3
Q31 2N3904 SOT23/SMD/NC
C601 1uF/NC
C602 1uF/NC
Trace width of 12V>30mil
Trace width of 5V >40mil
J1
7x1 DIP7/P2.0/NC
TXD:MT5351 Transmit
RXD:MT5351 Receiver
TXD1:MT5351& MT8205 Communication
RXD1:MT5351& MT8205 Communication
R1 10K
R2 10K
change 2/16
R354 0/NC
R355 0/NC
R356 0
R357 0
DV33B
SCL0 R3 0
SDA0 R4 0
LRCK R222 0/NC
DATA0 R230 0/NC
R229 0 LRCK
R228 0 DATA0
U30 74LVC245A
U31 74LVC245A
U32 74LVC245A
U33 74LVC245A
J24
CON50
FOR MT5351 INTERFACE
KAWA Confidential
Title
MT5351 INTERFACE
Size B
Document Number AKAI_MT8202_27US_LVDS_V0.0
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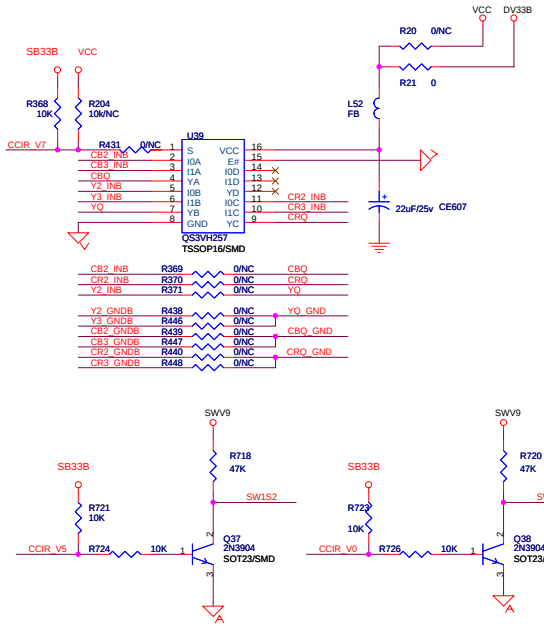
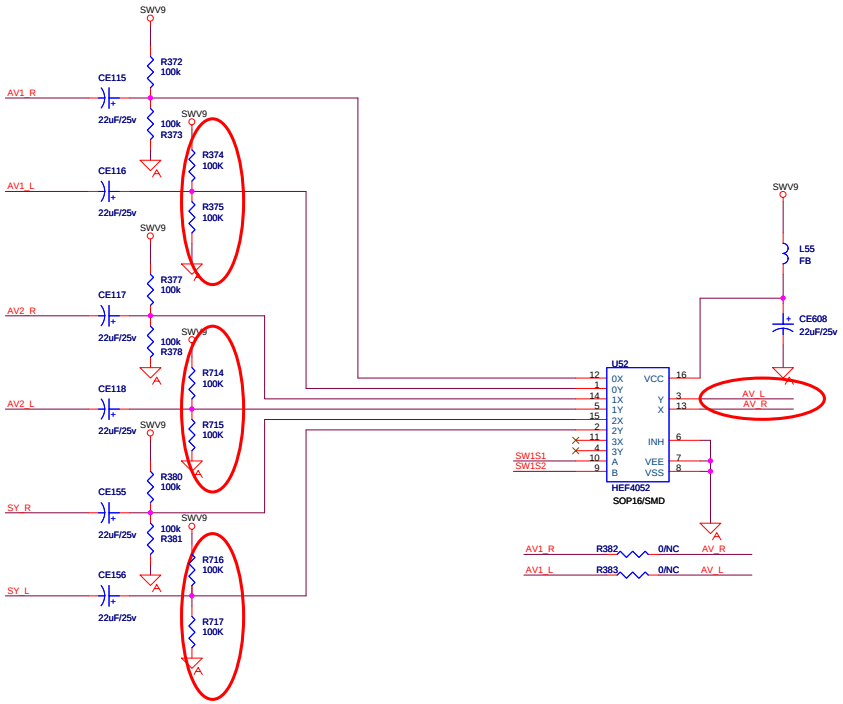
INPUT

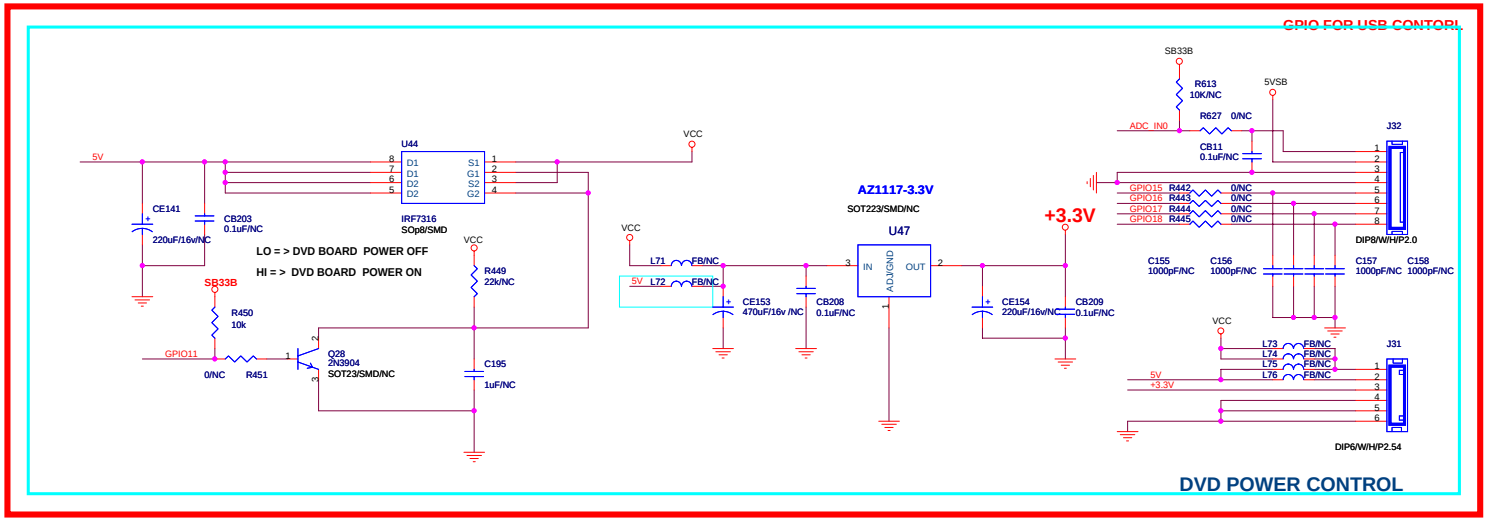
ADC_IN0	ADC_IN0	3
CCIR_V0	CCIR_V0	3
CCIR_V5	CCIR_V5	3
CCIR_V7	CCIR_V7	3
GPIO11	GPIO11	3
GPIO15	GPIO15	3
GPIO16	GPIO16	3
GPIO17	GPIO17	3
GPIO18	GPIO18	3
VFE_GND	VFE_GND	2,3,4,11
AADCVSS	AADCVSS	3,4,10
AV1_R	AV1_R	15
AV1_L	AV1_L	15
AV2_R	AV2_R	15
AV2_L	AV2_L	15
SY_R	SY_R	15
SY_L	SY_L	15
Y2_INB	Y2_INB	15
Y2_GNDB	Y2_GNDB	10,15
CB2_INB	CB2_INB	15
CB2_GNDB	CB2_GNDB	10,15
CR2_INB	CR2_INB	15
CR2_GNDB	CR2_GNDB	10,15
Y3_INB	Y3_INB	15
Y3_GNDB	Y3_GNDB	15
CB3_INB	CB3_INB	15
CB3_GNDB	CB3_GNDB	15
CR3_INB	CR3_INB	15
CR3_GNDB	CR3_GNDB	15
9V	9V	1,7,9,14

OUTPUT

AV_R	AV_R	9
AV_L	AV_L	9
YQ	YQ	10
CBQ	CBQ	10
CRQ	CRQ	10
YQ_GND	YQ_GND	10
CBQ_GND	CBQ_GND	10
CRQ_GND	CRQ_GND	10







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Title: DAUGHTER BOARD IN			
Size: C	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
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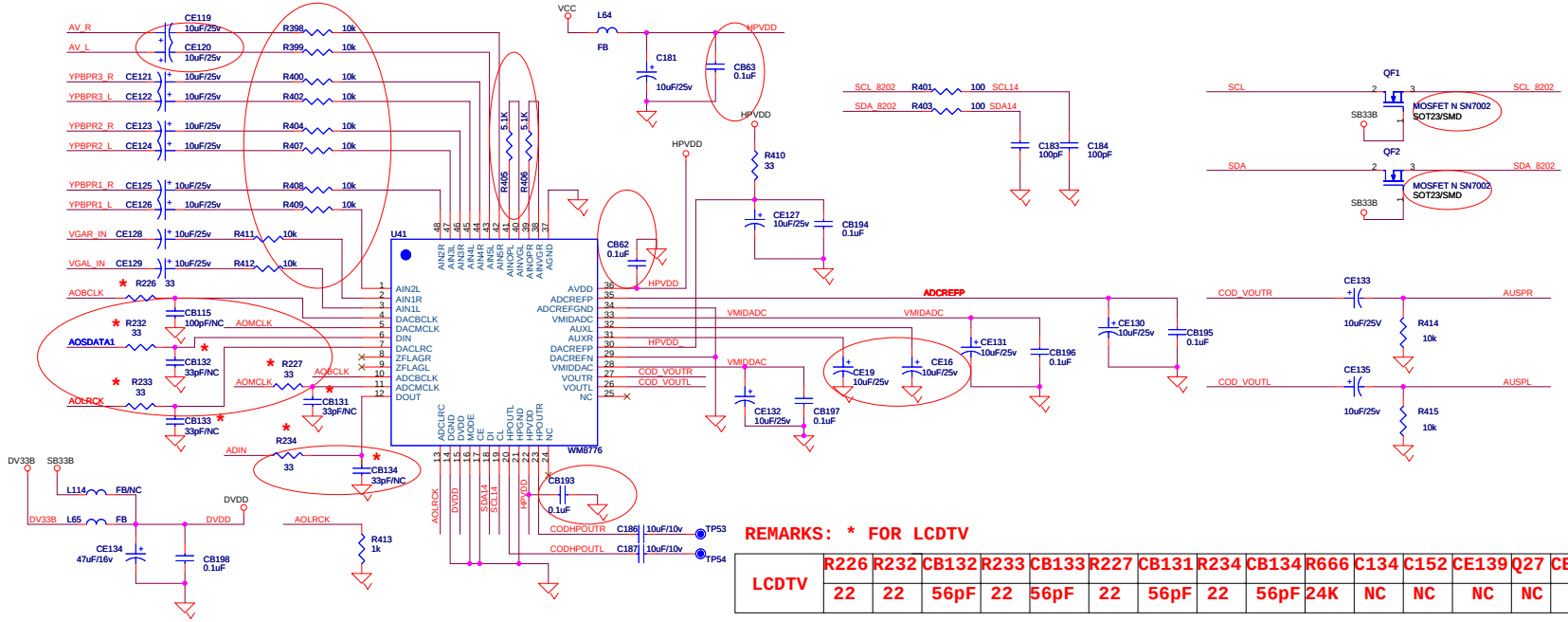
INPUT

GPIO7	GPIO7	3
SCL	SCL	1,14
SDA	SDA	1,14
SDA_8202	SDA_8202	3,6,12
SCL_8202	SCL_8202	3,6,12
AOSDATA1	AOSDATA1	3
AOMCLK	AOMCLK	3,16
AOBCLK	AOBCLK	3,16
AOLRCK	AOLRCK	3,16
ADIN	ADIN	3
AV_R	AV_R	8
AV_L	AV_L	8
YPBPR1_L	YPBPR1_L	15
YPBPR1_R	YPBPR1_R	15
YPBPR2_R	YPBPR2_R	15
YPBPR2_L	YPBPR2_L	15
YPBPR3_R	YPBPR3_R	15
YPBPR3_L	YPBPR3_L	15
VGAR_IN	VGAR_IN	11
VGAL_IN	VGAL_IN	11
TESTP2	TESTP2	3
AR	AR	3
AL	AL	3
MU	MU	16
A_MUTE	A_MUTE	17
9V	9V	1,7,14

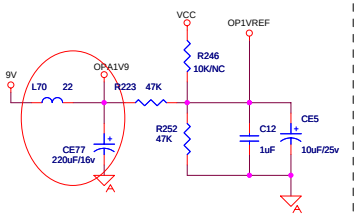
OUTPUT

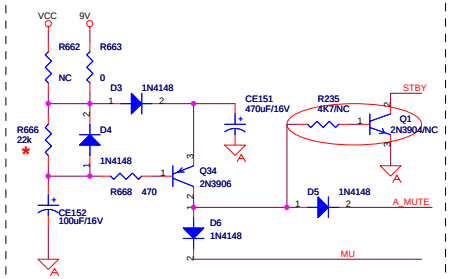
AUSPR	AUSPR	16
AUSPL	AUSPL	16
AVR_OUT	AVR_OUT	15
AVL_OUT	AVL_OUT	15
CVBS_OUT	CVBS_OUT	6,15

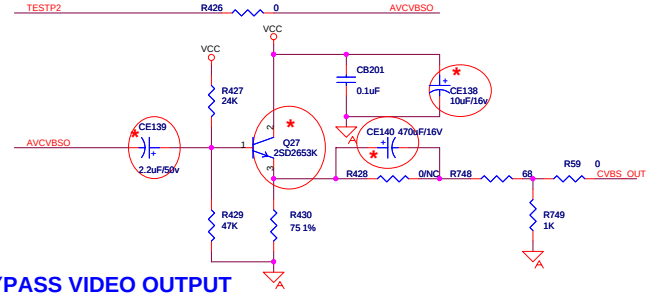


REMARKS: * FOR LCDTV

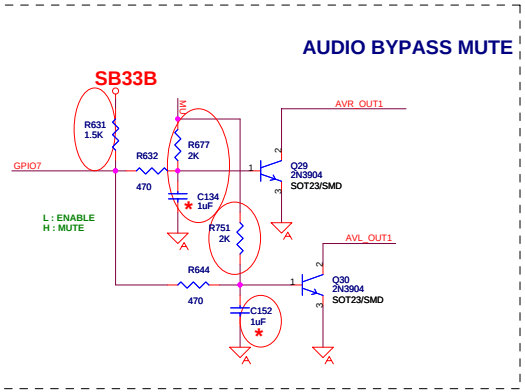
	R226	R232	CB132	R233	CB133	R227	CB131	R234	CB134	R666	C134	C152	CE139	Q27	CE140	CE138
LCDTV	22	22	56pF	22	56pF	22	56pF	22	56pF	24K	NC	NC	NC	NC	NC	NC

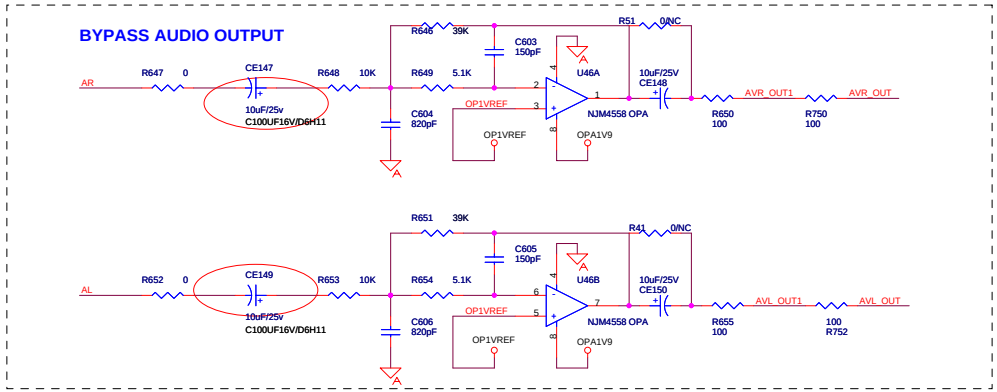






BYPASS VIDEO OUTPUT





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Title	M8776 & VIDEO BYPASS		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Saturday, April 22, 2006		Sheet 9	17

CVBS0 CVBS1 CVBS2

SY0 SC0

SY1 SC1

Y0+ Y0- PB0+ PB0- PR0+ PR0- SOY0

Y1+ Y1- PB1+ PB1- PR1+ PR1- SOY1

MPX1

MPX2

TO MT8202

TV_GND CVBS_0 SIF AF CVBS_1 CVBS1_GND CVBS_2 CVBS2_GND SY_1 SY_1_GND SC_1 SC_1_GND SY_0 SY_0_GND SC_0 SC_0_GND

SOY1 SOY0 Y1_INB Y1_GNDB CR1_INB CR1_GNDB CB1_INB CB1_GNDB CBQ CRQ YQ YQ_GND CBQ_GND CRQ_GND

FROM AV BOARD

AADCVSS

THIS PAGE NEARLY IC

CVBS_0 R197 0 C110 47nF CVBS0
C113 330pF TV_GND

CVBS_1 R200 0 C117 47nF CVBS1
C120 330pF CVBS1_GND

CVBS_2 R424 0 C188 47nF CVBS2
C189 330pF CVBS2_GND

SY_0 R198 0 C111 47nF SY0
C114 330pF SY_0_GND

SC_0 R201 0 C118 47nF SC0
C121 330pF SC_0_GND

SY_1 R205 0 C125 47nF SY1
C128 330pF SY_1_GND

SC_1 R209 0 C132 47nF SC1
C135 330pF SC_1_GND

R55 0 C112 4.7nF SOY0

YQ R199 68 C115 100nF Y0+
C116 15pF

YQ_GND R202 100 C119 100nF Y0-

CBQ R203 68 C122 100nF PB0+
C123 15pF

CBQ_GND R206 100 C126 100nF PB0-

CRQ R207 68 C129 100nF PR0+
C130 15pF

CRQ_GND R210 100 C133 100nF PR0-

R56 0 C136 4.7nF SOY1

Y1_INB R211 68 C137 100nF Y1+
C138 15pF

Y1_GNDB R213 100 C140 100nF Y1-

CB1_INB R214 68 C141 100nF PB1+
C142 15pF

CB1_GNDB R217 100 C145 100nF PB1-

CR1_INB R218 68 C146 100nF PR1+
C147 15pF

CR1_GNDB R219 100 C148 100nF PR1-

FROM Tuner

SIF R212 8.2K C139 10nF MPX1
C48 1.8pF AADCVSS

AF R215 39K R216 39K CE70 + 47uF/16V MPX2
C143 15pF C144 15pF AADCVSS

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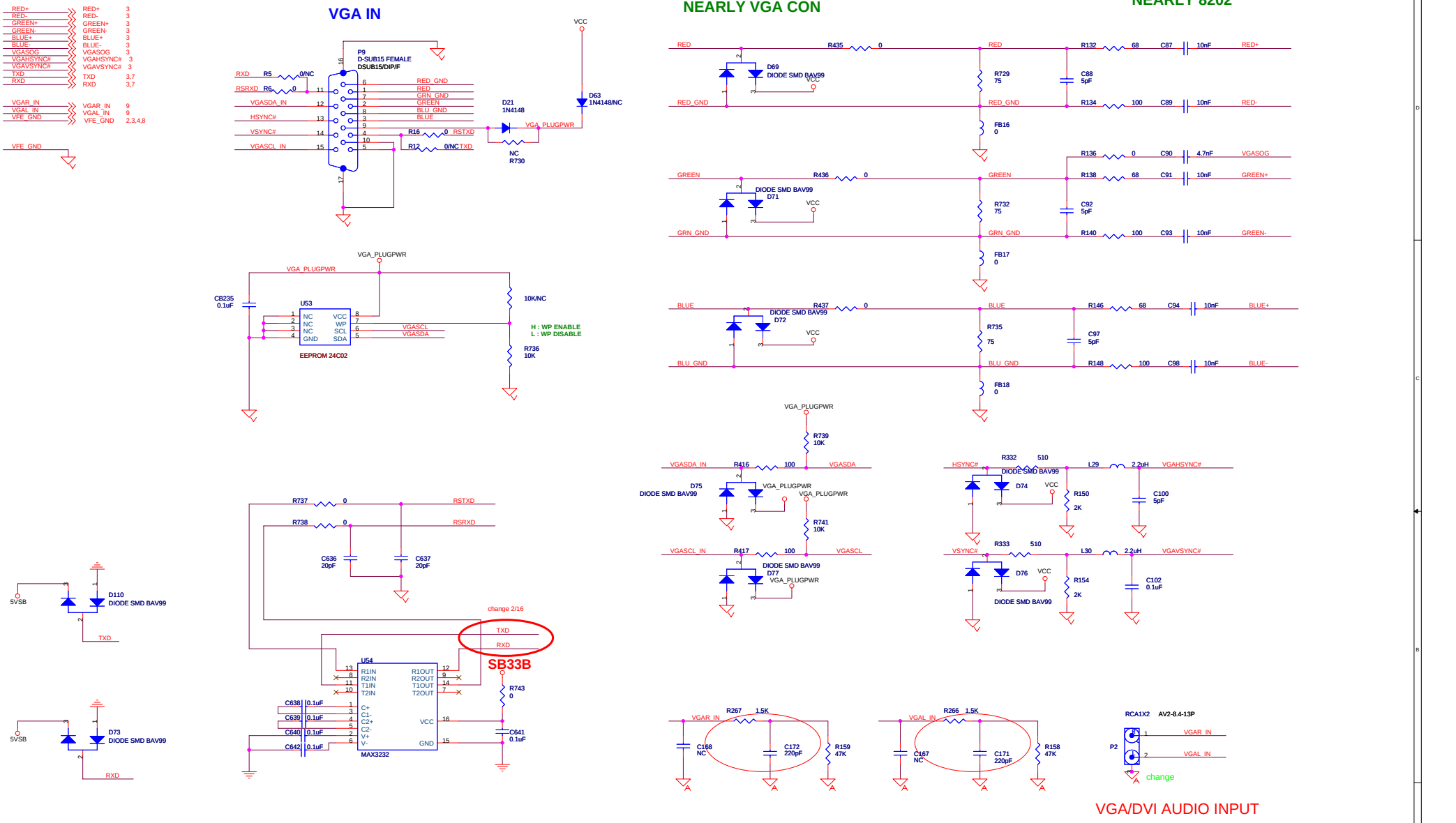
Title	AUDIO / VIDEO IN CIRCUIT		
Size C	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
Date: Thursday, April 13, 2006		Sheet 10	17


VGA IN
NEARLY VGA CON
NEARLY 8202
RED+ RED- GREEN+ GREEN- BLUE+ BLUE- VGASOG VGAHSYNC# VGAVSYNC# TXD RXD
VGAR_IN VGAL_IN VFE_GND
P9 D-SUB15 FEMALE DSUB15/DIP/F
RXD R5 0/NC
RSRXD R6 0
VGASDA_IN HSYNC# VSYNC# VGASCL_IN
RED_GND RED GRN_GND GREEN BLU_GND BLUE
R16 0 RSTXD
R12 0/NC TXD
D21 1N4148
VGA_PLUGPWR
NC R730
VCC
D63 1N4148/NC
CB235 0.1uF
U53
NC NC NC GND VCC WP SCL SDA
EEPROM 24C02
10K/NC
R736 10K
H : WP ENABLE
L : WP DISABLE
R737 0 RSTXD
R738 0 RSRXD
C636 20pF
C637 20pF
change 2/16
SB33B
U54
R1IN R2IN T1IN T2IN R1OUT R2OUT T1OUT T2OUT
C638 0.1uF
C639 0.1uF
C640 0.1uF
C642 0.1uF
C+ C1- C2+ C2- V+ V-
MAX3232
R743 0
C641 0.1uF
5VSB
D110 DIODE SMD BAV99
D73 DIODE SMD BAV99
TXD
RXD
RED R435 0
D69 DIODE SMD BAV99
R729 75
C88 5pF
R132 68 C87 10nF RED+
R134 100 C89 10nF RED-
FB16 0
GREEN R436 0
DIODE SMD BAV99 D71
R732 75
C92 5pF
R136 0 C90 4.7nF VGASOG
R138 68 C91 10nF GREEN+
R140 100 C93 10nF GREEN-
FB17 0
BLUE R437 0
DIODE SMD BAV99 D72
R735 75
C97 5pF
R146 68 C94 10nF BLUE+
R148 100 C98 10nF BLUE-
FB18 0
R739 10K
VGASDA_IN R416 100 VGASDA
D75 DIODE SMD BAV99
R741 10K
VGASCL_IN R417 100 VGASCL
D77 DIODE SMD BAV99
HSYNC# R332 510 L29 2.2uH VGAHSYNC#
D74 DIODE SMD BAV99
R150 2K
C100 5pF
VSYNC# R333 510 L30 2.2uH VGAVSYNC#
D76 DIODE SMD BAV99
R154 2K
C102 0.1uF
VGAR_IN R267 1.5K
C168 NC
C172 220pF
R159 47K
VGAL_IN R266 1.5K
C167 NC
C171 220pF
R158 47K
RCA1X2 AV2-8.4-13P
P2
change
VGA/DVI AUDIO INPUT
KAWA Confidential
Title
VGA IN & PC AUDIO IN
Size C
Document Number AKAI_MT8202_27US_LVDS_V0.0
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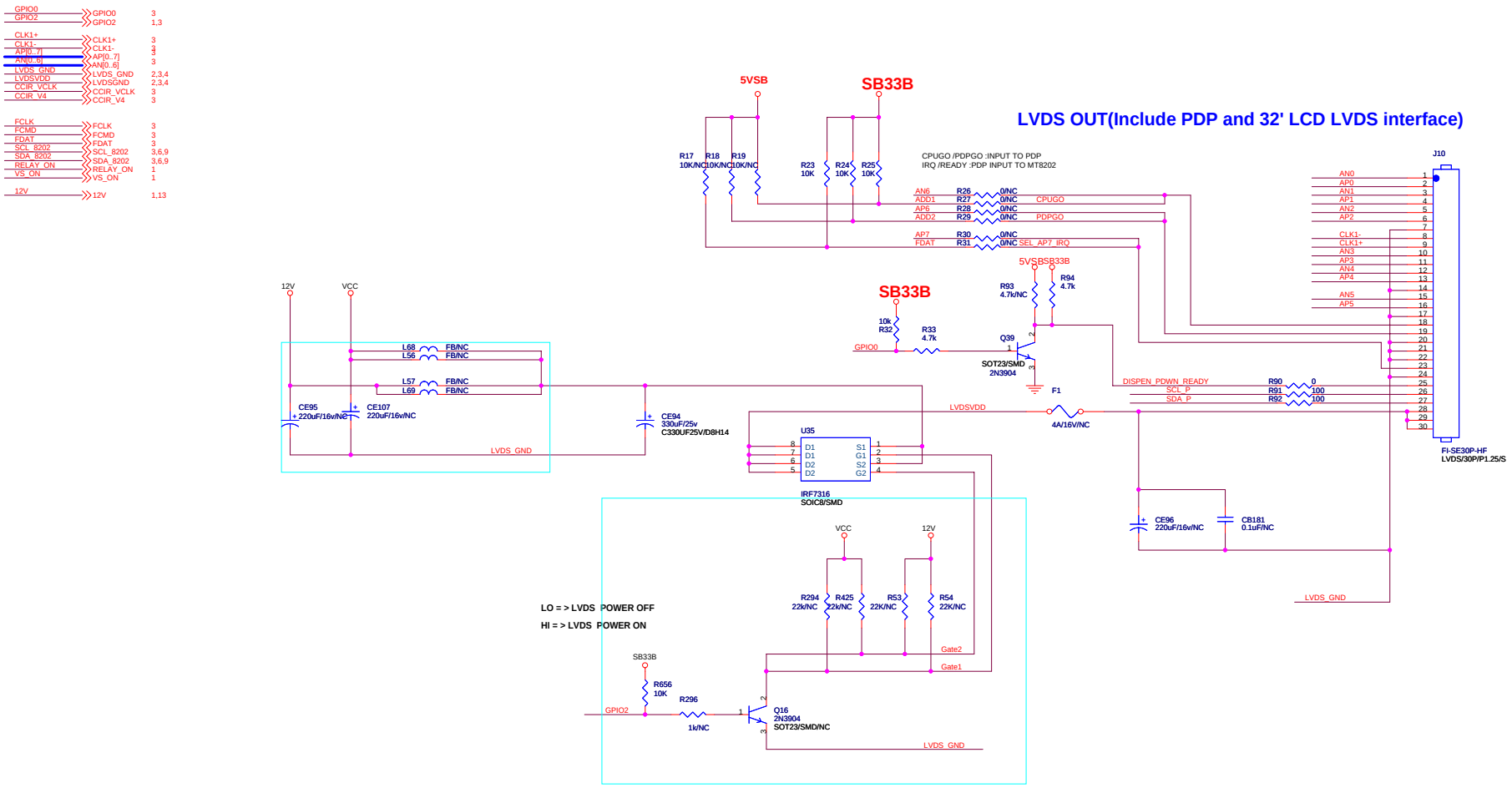

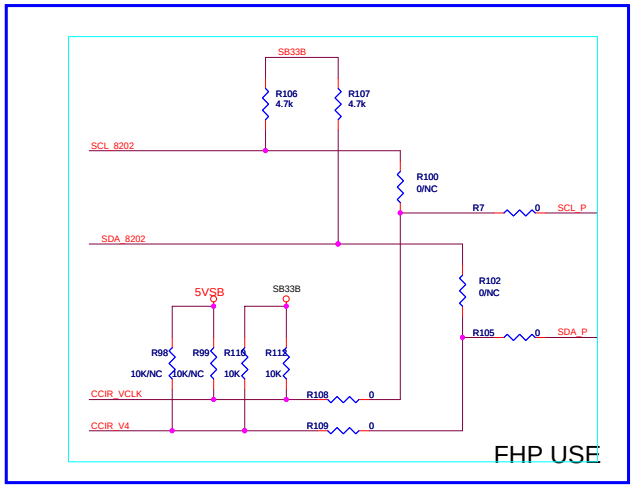

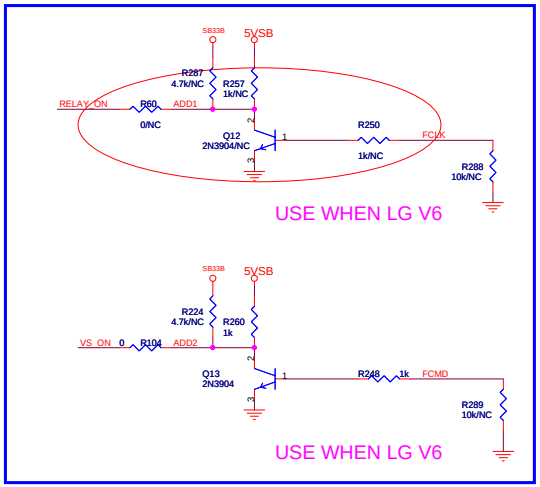

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Size: C	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
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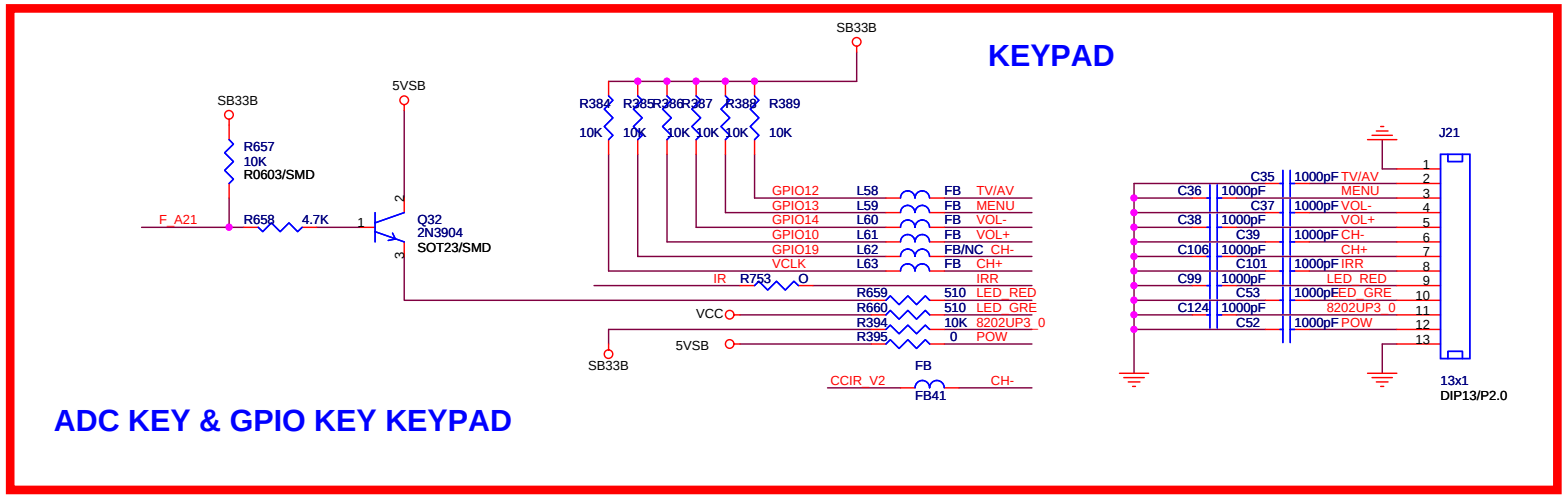
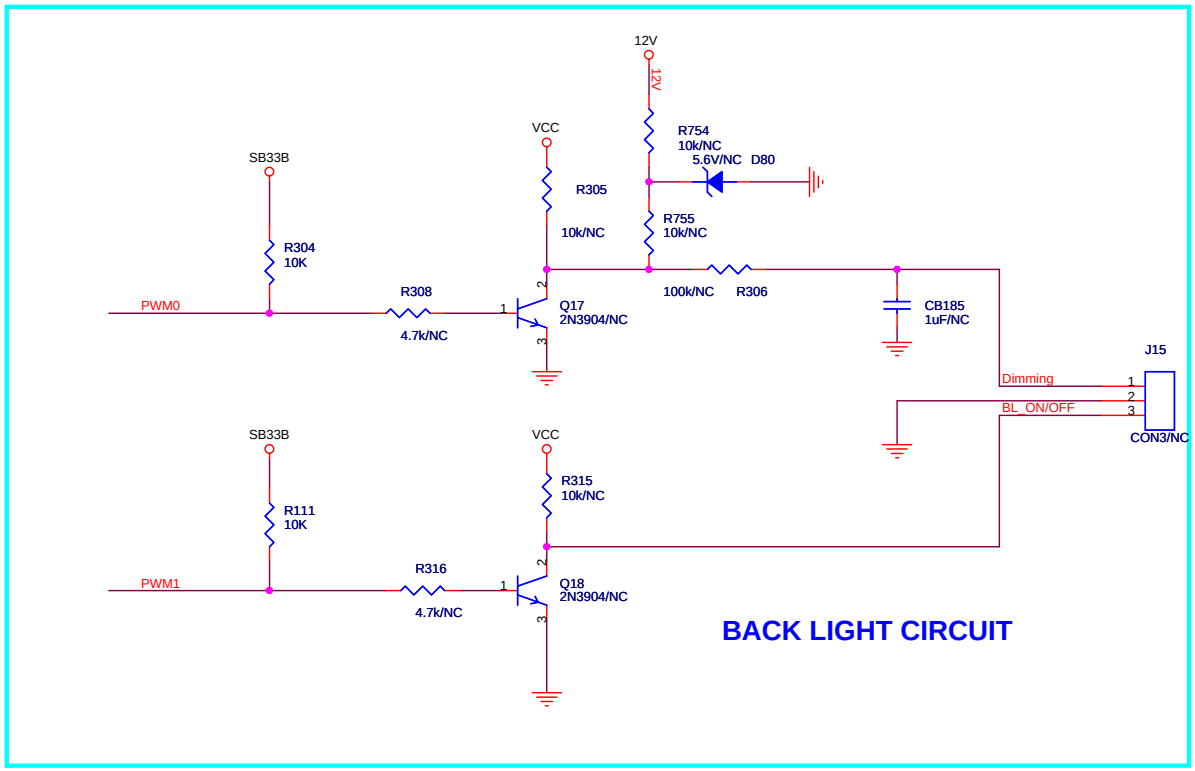
IR	IR	3,15
GPIO10	GPIO10	3
GPIO12	GPIO12	3
GPIO13	GPIO13	3
GPIO14	GPIO14	1,3
PWM0	PWM0	3
PWM1	PWM1	3
8202UP3_0	8202UP3_0	3
GPIO14	GPIO14	1,3
GPIO19	GPIO19	1,3
VCLK	VCLK	3
F_A21	F_A21	3
CCIR_V2	CCIR_V2	3
12V	12V	1,12





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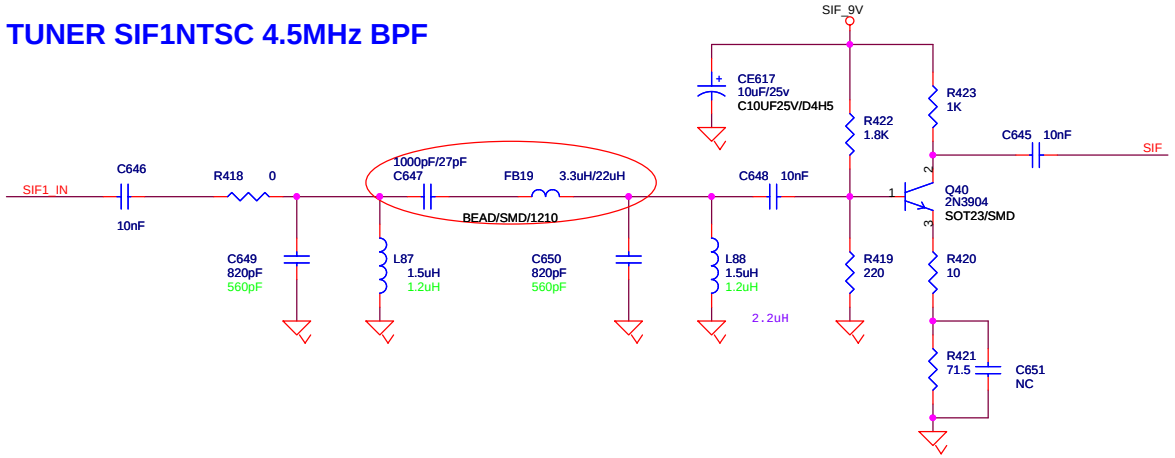
Title: BACK LIGHT / KEYPAD			
Size: B	Document Number: AKAI_MT8202_27US_LVDS_V0.0	<Designer>	Rev: 1
		Checked: <Checker>	
Date: Thursday, April 13, 2006		Sheet 13	17

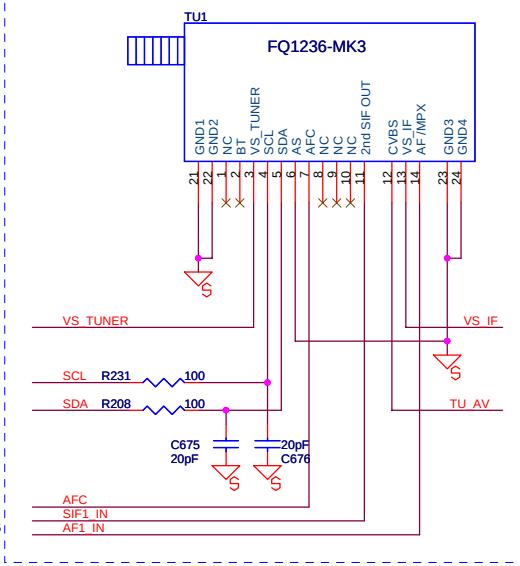
SCL 1,9
SDA 1,9
CVBS_0 10
TV_GND 10
AF 10
SIF 10
ADC_IN4 3
9V 1,7,9

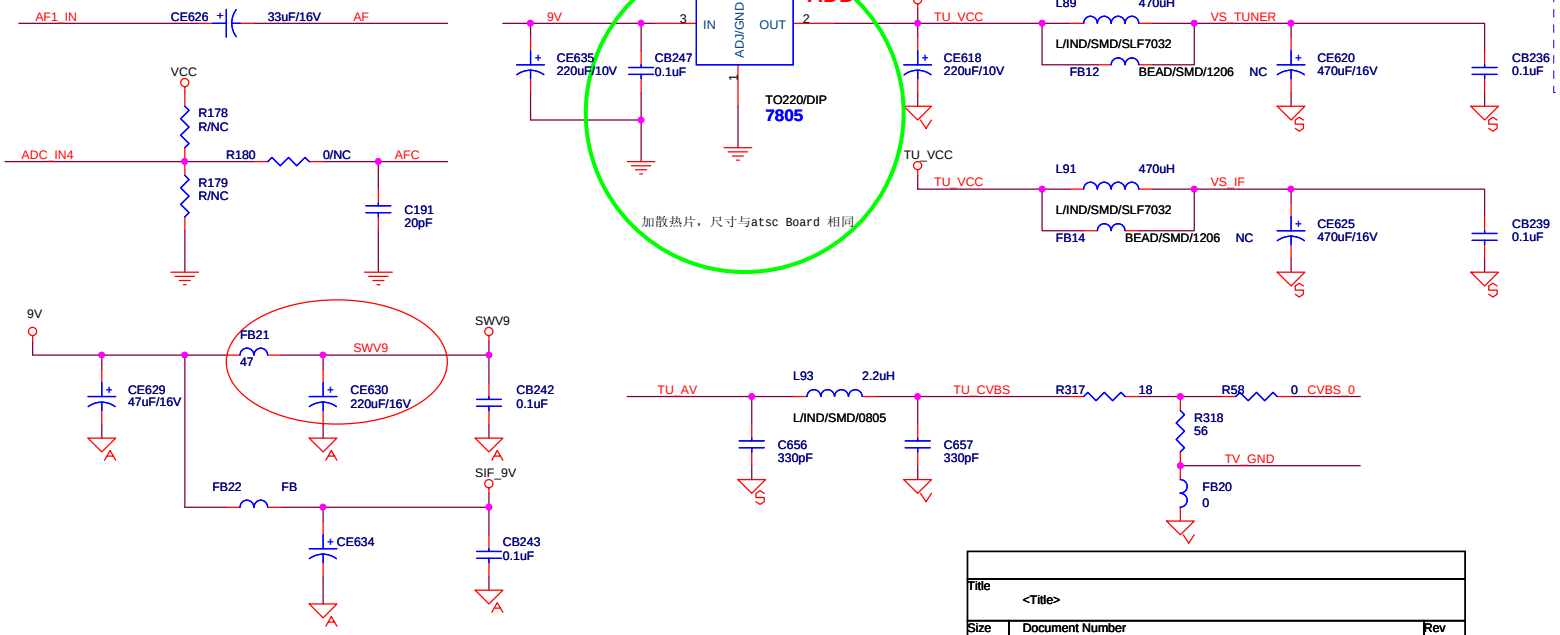
TUNER SIF1NTSC 4.5MHz BPF

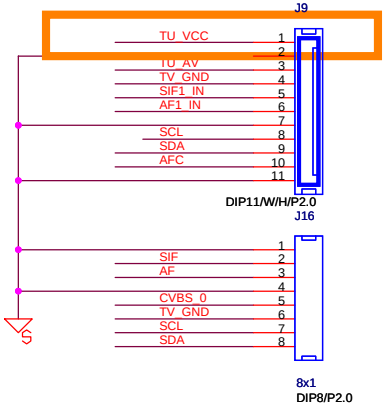


FQ1216 : PAL
FQ1236 : NTSC

ADDRESS
TUNER IF
C0 84







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Size Custom	Document Number <Doc>		Rev <RevCode>
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Title	TUNER IN		
Size Custom	Document Number AKAI_MT8202_27US_LVDS_V0.0	<Designer> Checked: <Checker>	Rev 1
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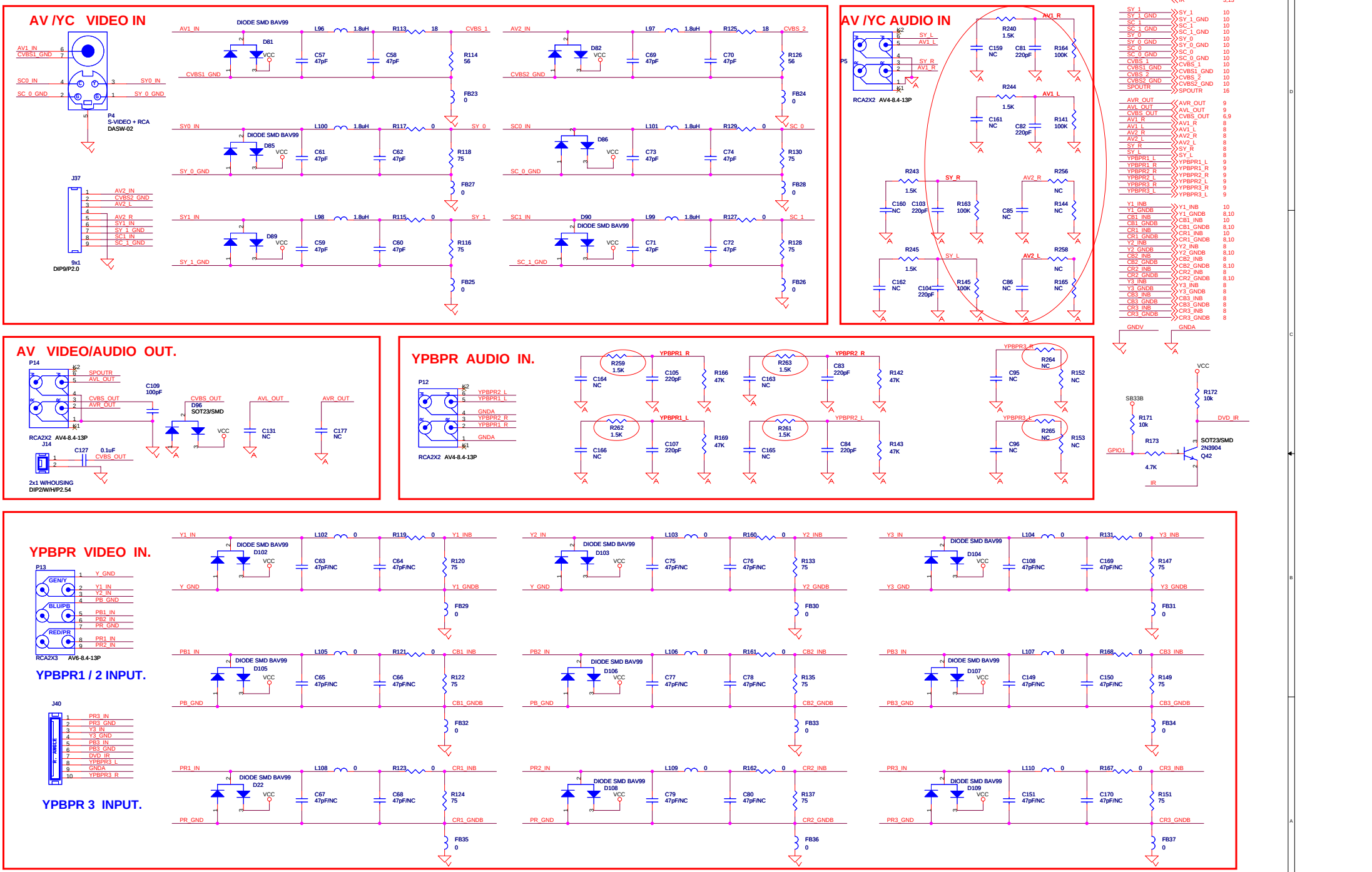
AV /YC VIDEO IN
AV1_IN
CVBS1_GND
SC0_IN
SC_0_GND
SY0_IN
SY_0_GND
P4
S-VIDEO + RCA
DASW-02
J37
AV2_IN
CVBS2_GND
AV2_L
AV2_R
SY1_IN
SY_1_GND
SC1_IN
SC_1_GND
9x1
DIP9/P2.0
DIODE SMD BAV99
D81
D82
D85
D86
D89
D90
VCC
L96
L97
L98
L99
L100
L101
1.8uH
R113
R125
R115
R127
R117
R129
18
0
CVBS_1
CVBS_2
SY_0
SC_0
SY_1
SC_1
R114
R126
R118
R130
R116
R128
56
75
FB23
FB24
FB27
FB28
FB25
FB26
C57
C69
C61
C73
C59
C71
C58
C70
C62
C74
C60
C72
47pF
AV /YC AUDIO IN
RCA2X2 AV4-8.4-13P
SY_L
AV1_L
SY_R
AV1_R
R240
1.5K
R244
R243
R245
C159
C81
R164
C161
C82
R141
C160
C103
R163
C85
R144
C162
C104
R145
C86
R165
220pF
100K
NC
R256
R258
AV /VIDEO/AUDIO OUT.
P14
SPOUTR
AVL_OUT
CVBS_OUT
AVR_OUT
C109
100pF
D96
SOT23/SMD
C131
C177
J14
C127
0.1uF
2x1 W/HOUSING
DIP2/W/H/P2.54
YPBPR AUDIO IN.
P12
YPBPR2_L
YPBPR1_L
GNDA
YPBPR2_R
YPBPR1_R
R259
R262
R263
R261
R264
R265
C164
C166
C105
C107
C163
C165
C83
C84
C95
C96
R166
R169
R142
R143
R152
R153
47K
YPBPR VIDEO IN.
P13
GEN/Y
BLU/PB
RED/PR
Y_GND
Y1_IN
Y2_IN
PB_GND
PB1_IN
PB2_IN
PR_GND
PR1_IN
PR2_IN
RCA2X3 AV6-8.4-13P
YPBPR1 / 2 INPUT.
J40
PR3_IN
PR3_GND
Y3_IN
Y3_GND
PB3_IN
PB3_GND
DVD_IR
YPBPR3_L
GNDA
YPBPR3_R
YPBPR 3 INPUT.
D102
D103
D104
D105
D106
D107
D108
D109
D22
C63
C75
C108
C65
C77
C149
C67
C79
C151
C64
C76
C169
C66
C78
C150
C68
C80
C170
47pF/NC
R120
R133
R147
R122
R135
R149
R124
R137
R151
Y1_GNDB
Y2_GNDB
Y3_GNDB
CB1_GNDB
CB2_GNDB
CB3_GNDB
CR1_GNDB
CR2_GNDB
CR3_GNDB
FB29
FB30
FB31
FB32
FB33
FB34
FB35
FB36
FB37
GPIO1
IR
SY_1
SY_1_GND
SC_1
SC_1_GND
SY_0
SY_0_GND
SC_0
SC_0_GND
CVBS_1
CVBS1_GND
CVBS_2
CVBS2_GND
SPOUTR
AVR_OUT
AVL_OUT
CVBS_OUT
AV1_R
AV1_L
AV2_R
AV2_L
SY_R
SY_L
YPBPR1_L
YPBPR1_R
YPBPR2_R
YPBPR2_L
YPBPR3_R
YPBPR3_L
Y1_INB
Y1_GNDB
CB1_INB
CB1_GNDB
CR1_INB
CR1_GNDB
Y2_INB
Y2_GNDB
CB2_INB
CB2_GNDB
CR2_INB
CR2_GNDB
Y3_INB
Y3_GNDB
CB3_INB
CB3_GNDB
CR3_INB
CR3_GNDB
GNDV
GNDA
VCC
R172
10k
SB33B
R171
10k
DVD_IR
R173
SOT23/SMD
2N3904
Q42
4.7K
IR
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Title
AV IN
Size
C
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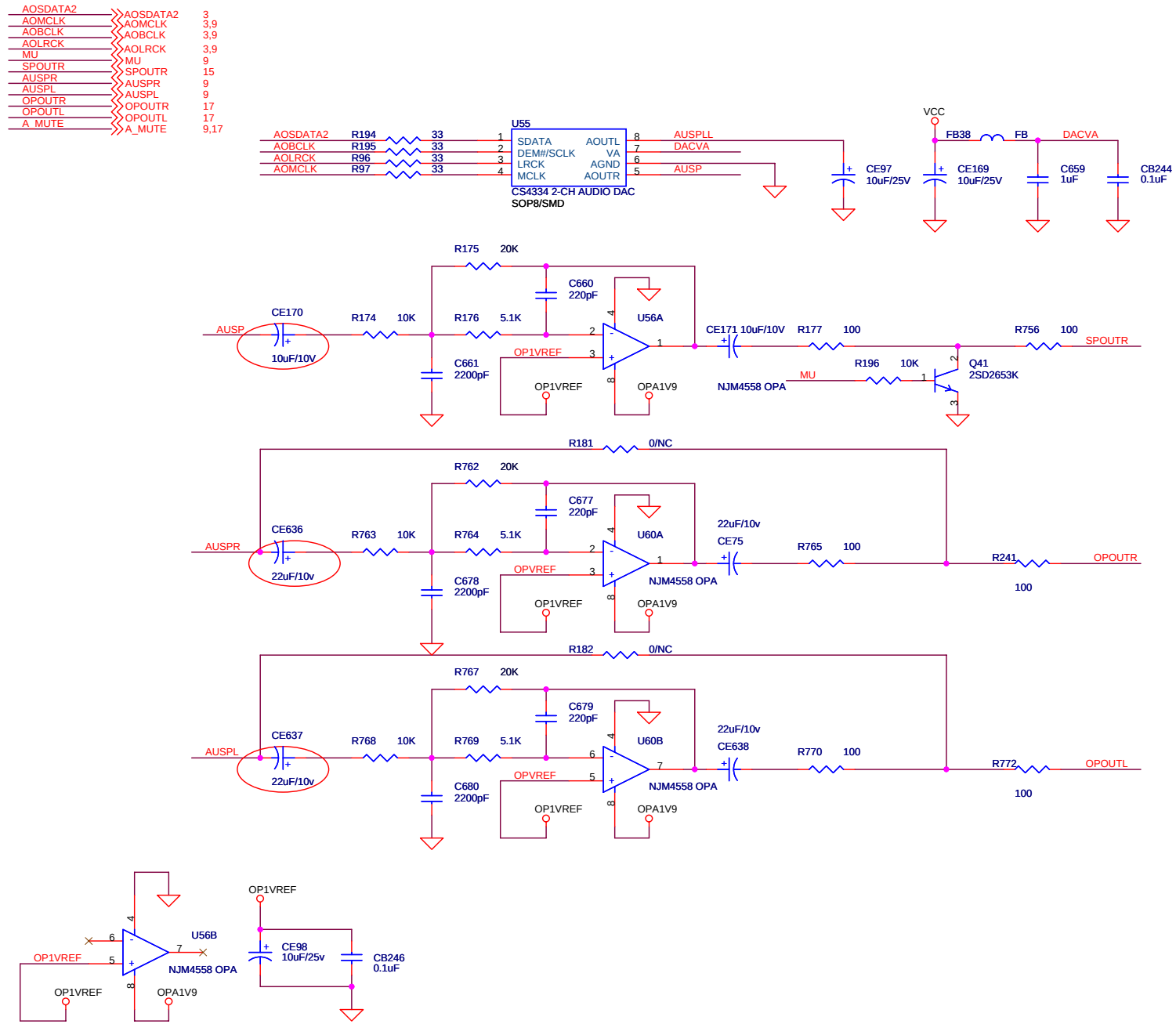

GPIO DECRIPTION

UP3_4 : SW SCL
UP3_5 : SW SDA
ERO0/UP3_0 :KEYPAD POWER
ERO1/UP3_1 : MAIN POWER SWITCH
VCLK : KEPAD CH+
GPIO19 : KEPAD CH-
DE/GPIO : DVD IR
CCIR_CLK : PDP USE
CCIR_V4 : PDP USE
GPIO0 : PDP USE
GPIO1 : NO USE
GPIO2 : LVDS POWER SW
GPIO3 : DTV POWER CONTROL
GPIO4 : EEPROM WRITE PROTECT
GPIO5/TXD : 2nd UART FOR MT5351
GPIO6/RXD : 2nd UART FOR MT5351
GPIO7 : AUDIO BYPASS MUTE CONTROL
GPIO8 : SPEAKER SWITCH
GPIO9 : AUDIO MUTE
GPIO10 : Indicates active video at HDMI port
GPIO11 : DVD POWER CONTROL
GPIO12 : AV SWITCH
GPIO13 : HDMI Hot Plug Detect
GPIO14 : NO USE
GPIO[15..18] : FOR DVD CONTROL
GPIO/PWM0 : DIMMING
GPIO/PWM1 : BACKLIGHT ON/OFF
OUT_27Mhz/GPIO : HDMI CRYSTAL
SDA1 : TO MT5351 I/F REQUEST
SCL1 : TO MT5351 I/F READY
F_A21 : KEYPAD(LED RED)
ADCIN0 : KEYPAD
ADCIN3:PDP 5VD DETECT
ADCIN4:FOR TUNER AFC

CCIR_V[0-3] : KEYPAD
CCIR_V5 : AUDIO SWITCH
CCIR_V6 : RESET DTV
CCIR_V7 : YPBPR VIDEO SWITCH

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Title: SUB WOOFER			
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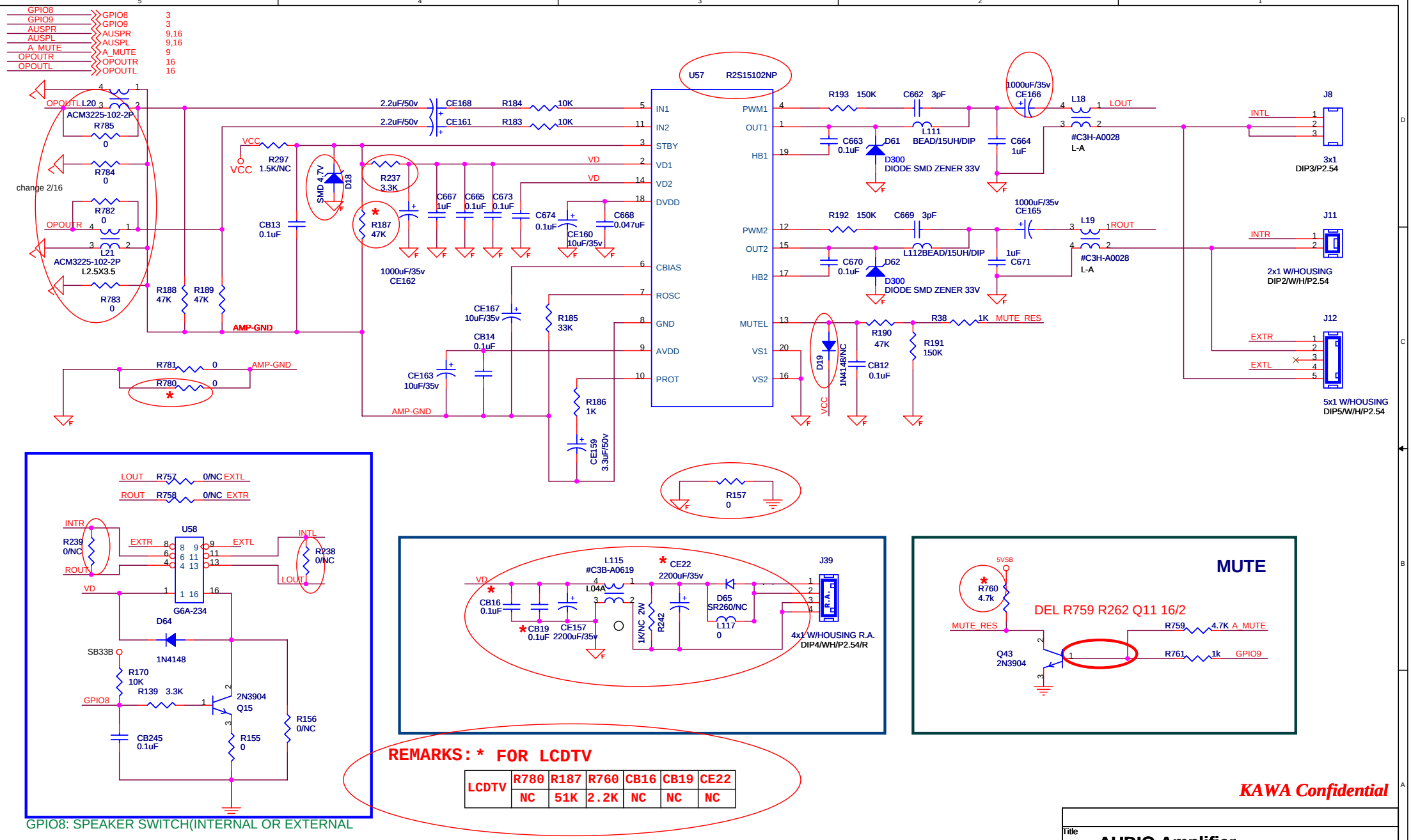
GPIO8 3
GPIO9 3
AUSPR 9,16
AUSPL 9,16
A_MUTE 9
OPOUTR 16
OPOUTL 16
U57 R2S15102NP
ACM3225-102-2P
R785 0
R784 0
R782 0
R783 0
ACM3225-102-2P
L2.5X3.5
change 2/16
R188 47K
R189 47K
AMP-GND
VCC
R297 1.5K/NC
SMD 4.7V
D18
CB13 0.1uF
R237 3.3K
R187 47K
1000uF/35v CE162
2.2uF/50v CE168
2.2uF/50v CE161
R184 10K
R183 10K
C667 1uF
C665 0.1uF
C673 0.1uF
C674 0.1uF
CE160 10uF/35v
C668 0.047uF
CE167 10uF/35v
CB14 0.1uF
CE163 10uF/35v
R185 33K
R186 1K
CE159 3.3uF/50v
IN1
IN2
STBY
VD1
VD2
DVDD
CBIAS
ROSC
GND
AVDD
PROT
PWM1
OUT1
HB1
PWM2
OUT2
HB2
MUTEL
VS1
VS2
R193 150K
C662 3pF
C663 0.1uF
D61
L111 BEAD/15UH/DIP
D300 DIODE SMD ZENER 33V
1000uF/35v CE166
C664 1uF
L18
LOUT
#C3H-A0028 L-A
R192 150K
C669 3pF
C670 0.1uF
D62
L112BEAD/15UH/DIP
1000uF/35v CE165
1uF C671
L19
ROUT
#C3H-A0028 L-A
D19 1N4148/NC
CB12 0.1uF
R38 1K MUTE_RES
R190 47K
R191 150K
J8
INTL
3x1 DIP3/P2.54
J11
INTR
2x1 W/HOUSING DIP2/W/H/P2.54
J12
EXTR
EXTL
5x1 W/HOUSING DIP5/W/H/P2.54
R781 0
R780 0
R157 0
LOUT R757 0/NC EXTL
ROUT R758 0/NC EXTR
U58
INTR
EXTR
EXTL
INTL
R239 0/NC
R238 0/NC
ROUT
LOUT
VD
G6A-234
D64
1N4148
SB33B
R170 10K
R139 3.3K
GPIO8
2N3904 Q15
R156 0/NC
R155 0
CB245 0.1uF
L115 #C3B-A0619
L04A
CE22 2200uF/35v
CB16 0.1uF
CB19 0.1uF
CE157 2200uF/35v
1K/NC 2W
R242
D65 SR260/NC
L117 0
J39
R.A.
4x1 W/HOUSING R.A. DIP4/WH/P2.54/R
5VSB
R760 4.7k
MUTE_RES
MUTE
DEL R759 R262 Q11 16/2
Q43 2N3904
R759 4.7K A_MUTE
R761 1k GPIO9
GPIO8: SPEAKER SWITCH(INTERNAL OR EXTERNAL
REMARKS: * FOR LCDTV
LCDTV | R780 | R187 | R760 | CB16 | CB19 | CE22
NC | 51K | 2.2K | NC | NC | NC
KAWA Confidential
Title AUDIO Amplifier
Size B
Document Number AKAI_MT8202_27US_LVDS_V0.0
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Rev 1
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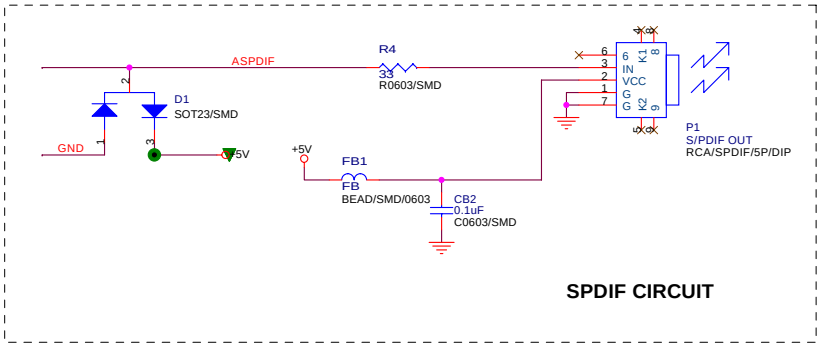
MT5111 / MT5351 REFERENCE DESIGN - 4 LAYERS

Rev	History	P#	DATE
RA-V1	INITIAL VERSION		2005/06/15
RA-V2	ADDED AUDIO SWITCH / REFINE POWER CIRCUIT		2005/07/14

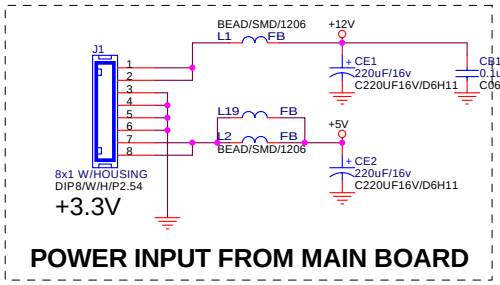
01. INDEX AND INTERFACE
02. POWER
03. TUNER
04. MT5111 ASIC
05. MT5351 ASIC
06. MT5351 PERIPHERAL
07. DDR MEMORY
08. NOR FLASH / JTAG / UART

NS : NON-STUFF

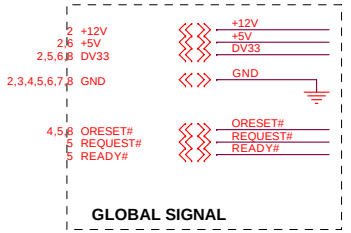
NAME	TYPE	DEVICE
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5V_tuner	POWER +5V	TUNER POWER
DV33_DM	POWER +3V3	MT5111 POWER
DV18	POWER +1V8	MT5111 POWER
DV33	POWER +3V3	MT5351 POWER
AV33	POWER +3V3	MT5351 ANALOG POWER
DV25	POWER +2V5	MT5351 DDR POWER
DV12	POWER +1V2	MT5351 POWER
GND	GROUND	GROUND

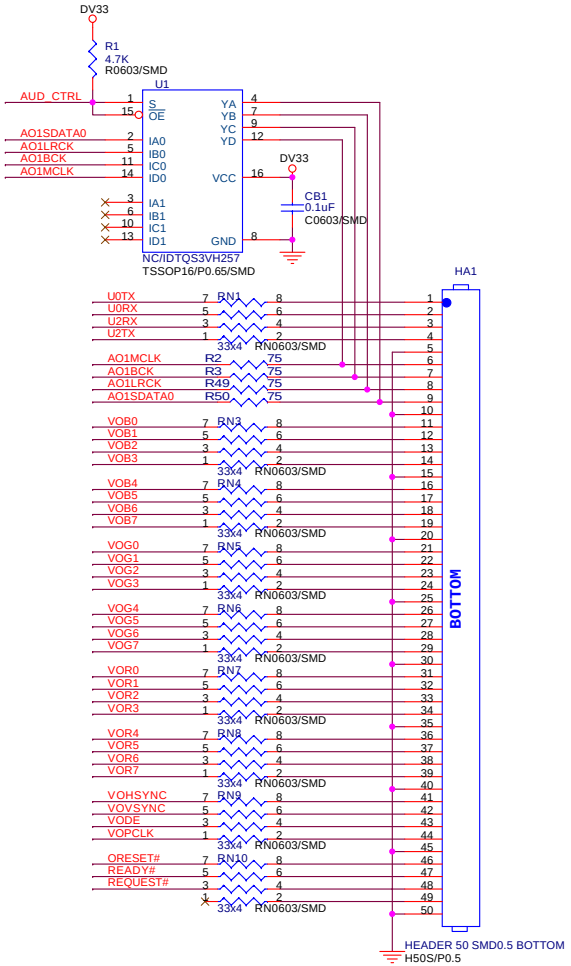


SPDIF CIRCUIT

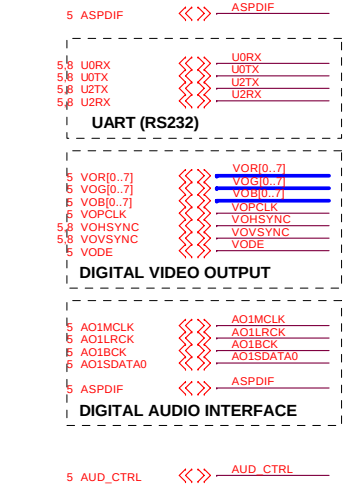


POWER INPUT FROM MAIN BOARD





DIGITAL OUTPUT



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Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
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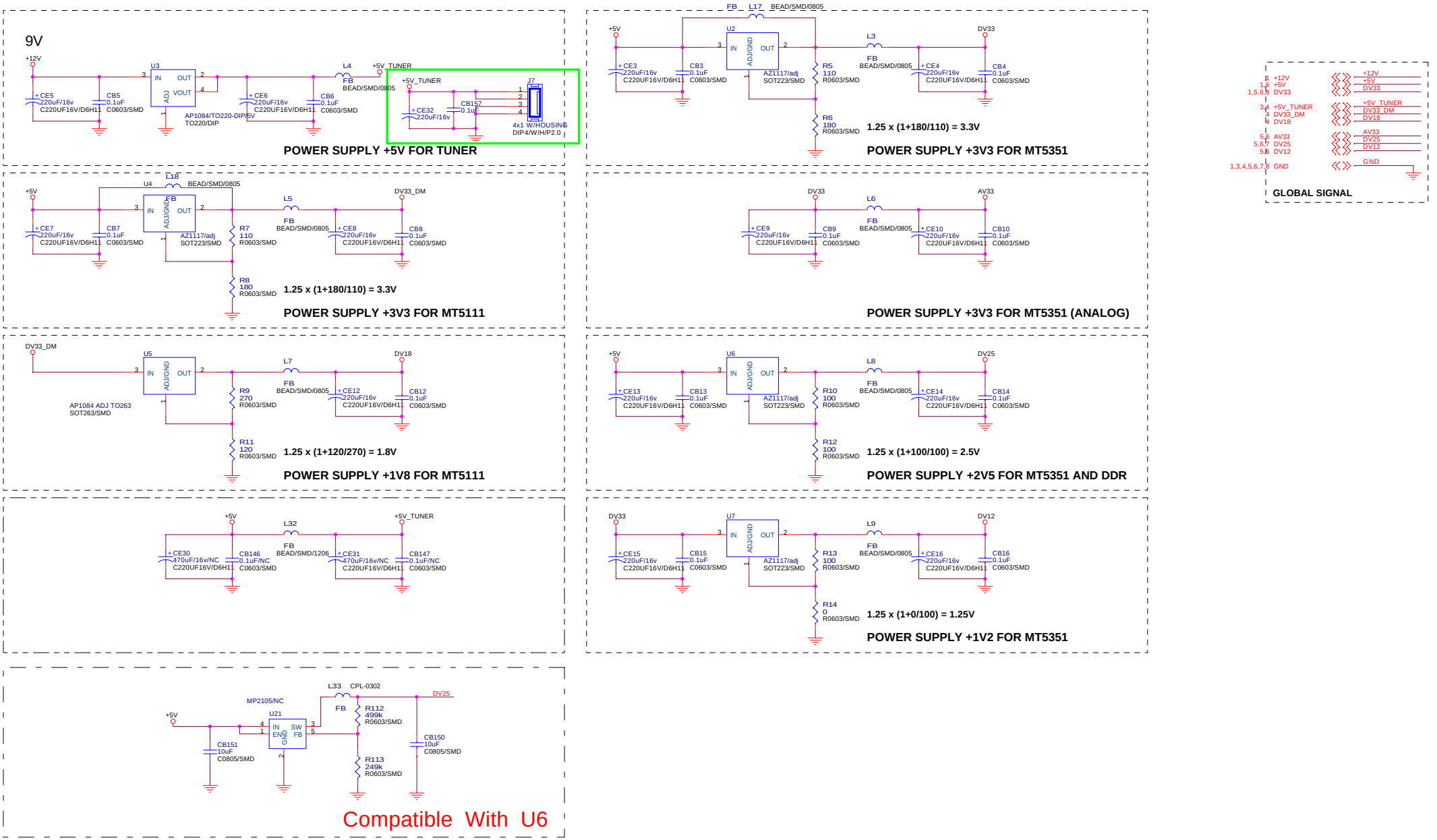

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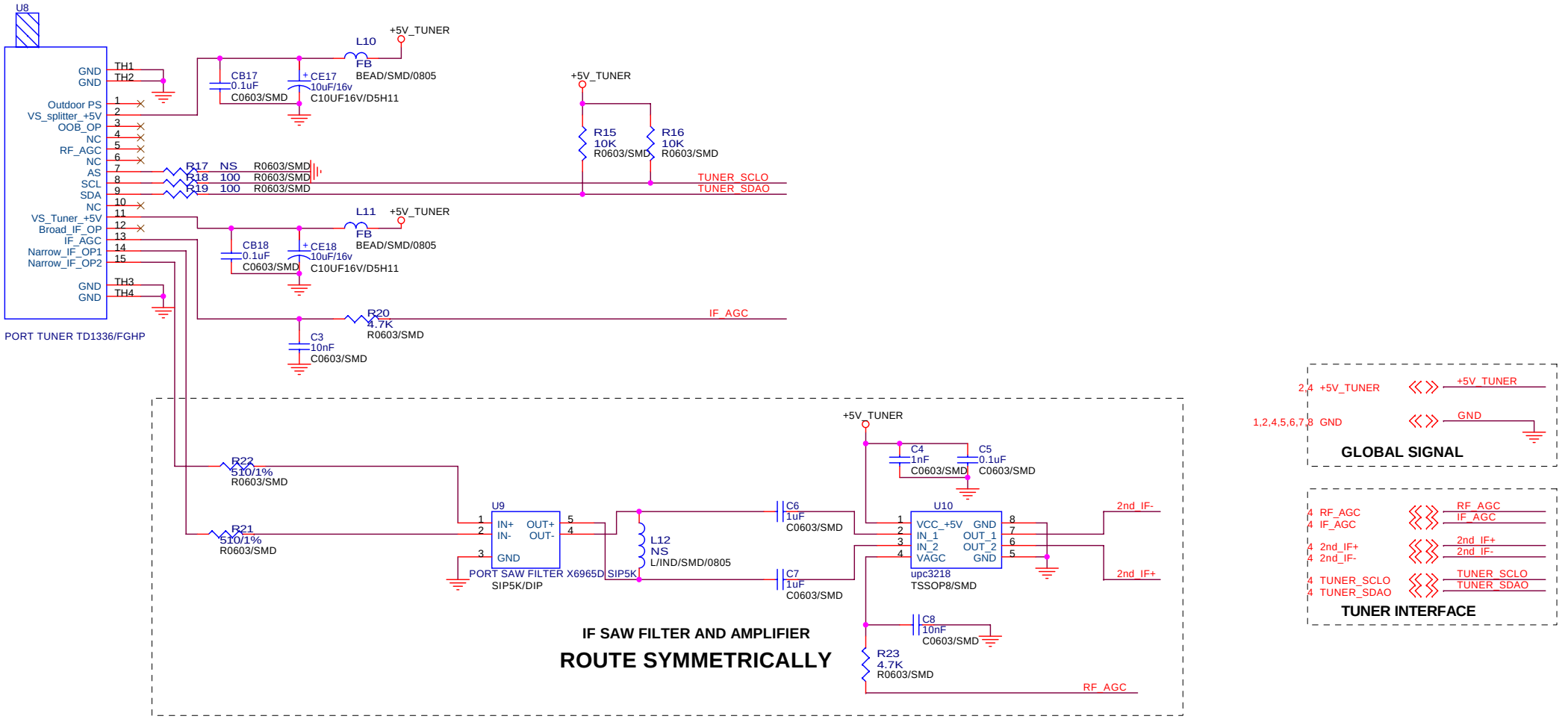
Title: POWER		
Size: Custom	Document Number: MT5351RA-V2	Rev: 1
Date: Monday, February 20, 2006	Sheet 2 of 8	TwinSon Chan



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Title: TUNER			
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
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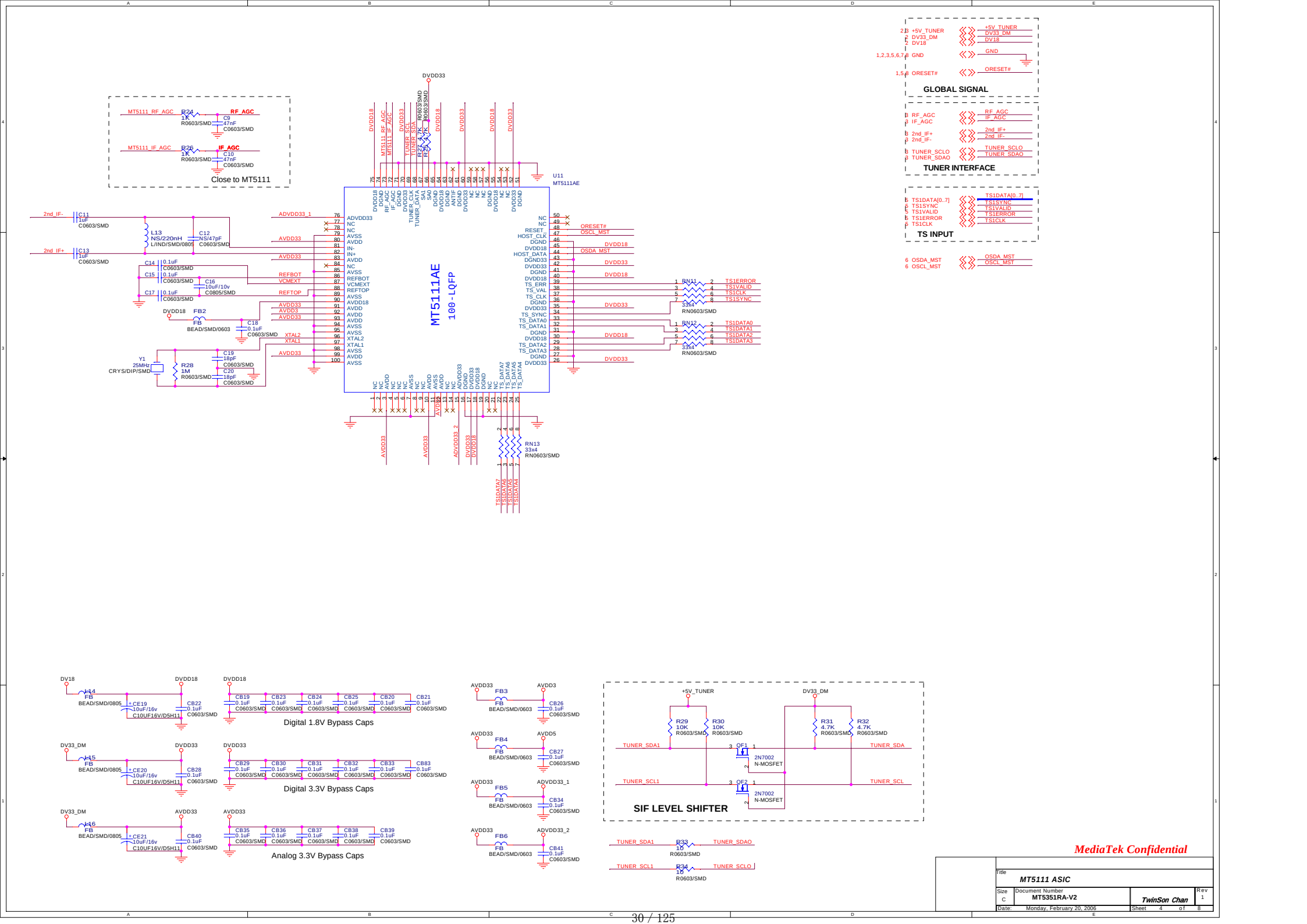
MT5111_RF_AGC
R24
1K
R0603/SMD
RF_AGC
C9
47nF
C0603/SMD
MT5111_IF_AGC
R26
1K
R0603/SMD
IF_AGC
C10
47nF
C0603/SMD
Close to MT5111
DVDD33
U11
MT5111AE
MT5111AE
100-LQFP
2nd_IF-
2nd_IF+
C11
1uF
C0603/SMD
L13
NS/220nH
L/IND/SMD/0805
C12
NS/47pF
C0603/SMD
C13
1uF
C0603/SMD
C14
0.1uF
C0603/SMD
C15
0.1uF
C0603/SMD
C16
10uF/10v
C0805/SMD
C17
0.1uF
C0603/SMD
REFBOT
VCMEXT
REFTOP
DVDD18
FB2
FB
BEAD/SMD/0603
C18
0.1uF
C0603/SMD
XTAL2
XTAL1
Y1
25MHz
CRYS/DIP/SMD
R28
1M
R0603/SMD
C19
18pF
C0603/SMD
C20
18pF
C0603/SMD
ADVDD33_1
ADVDD33_2
ORESET#
OSCL_MST
OSDA_MST
TS1ERROR
TS1VALID
TS1CLK
TS1SYNC
TS1DATA0
TS1DATA1
TS1DATA2
TS1DATA3
RN11
RN12
RN13
33x4
RN0603/SMD
+5V_TUNER
DV33_DM
DV18
GND
ORESET#
GLOBAL SIGNAL
RF_AGC
IF_AGC
2nd_IF+
2nd_IF-
TUNER_SCLO
TUNER_SDAO
TUNER INTERFACE
TS1DATA[0..7]
TS1SYNC
TS1VALID
TS1ERROR
TS1CLK
TS INPUT
DV18
DVDD18
FB4
BEAD/SMD/0805
CE19
10uF/16v
C10UF16V/D5H11
CB22
0.1uF
C0603/SMD
CB19
CB23
CB24
CB25
CB20
CB21
Digital 1.8V Bypass Caps
DV33_DM
DVDD33
FB5
CE20
CB28
CB29
CB30
CB31
CB32
CB33
CB83
Digital 3.3V Bypass Caps
AVDD33
FB6
CE21
CB40
CB35
CB36
CB37
CB38
CB39
Analog 3.3V Bypass Caps
AVDD3
AVDD5
ADVDD33_1
ADVDD33_2
FB3
CB26
CB27
CB34
CB41
SIF LEVEL SHIFTER
+5V_TUNER
DV33_DM
R29
10K
R30
10K
R31
4.7K
R32
4.7K
TUNER_SDA1
TUNER_SCL1
TUNER_SDA
TUNER_SCL
Q1
Q2
2N7002
N-MOSFET
R33
10
R34
10
TUNER_SDAO
TUNER_SCLO
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MT5111 ASIC
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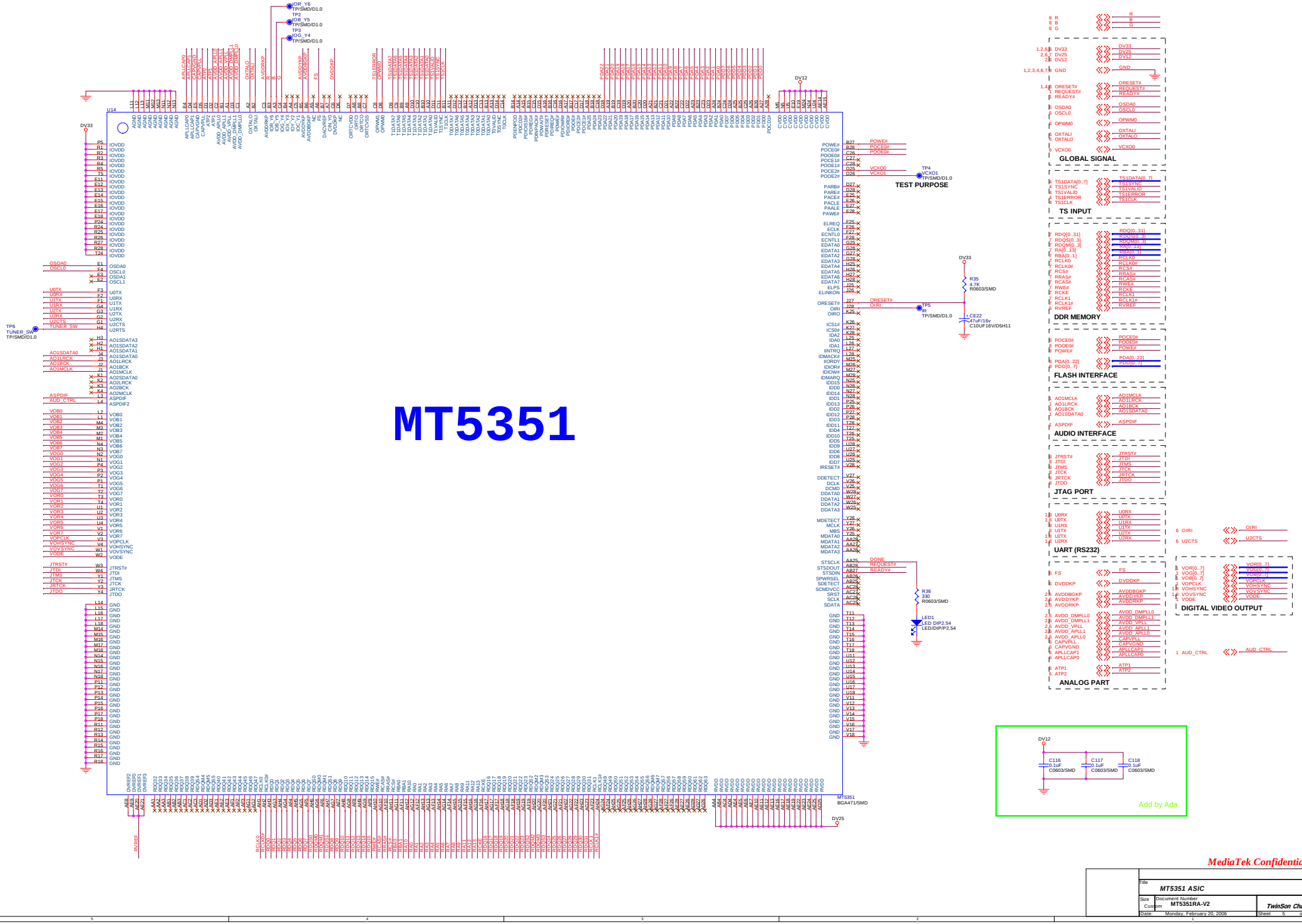
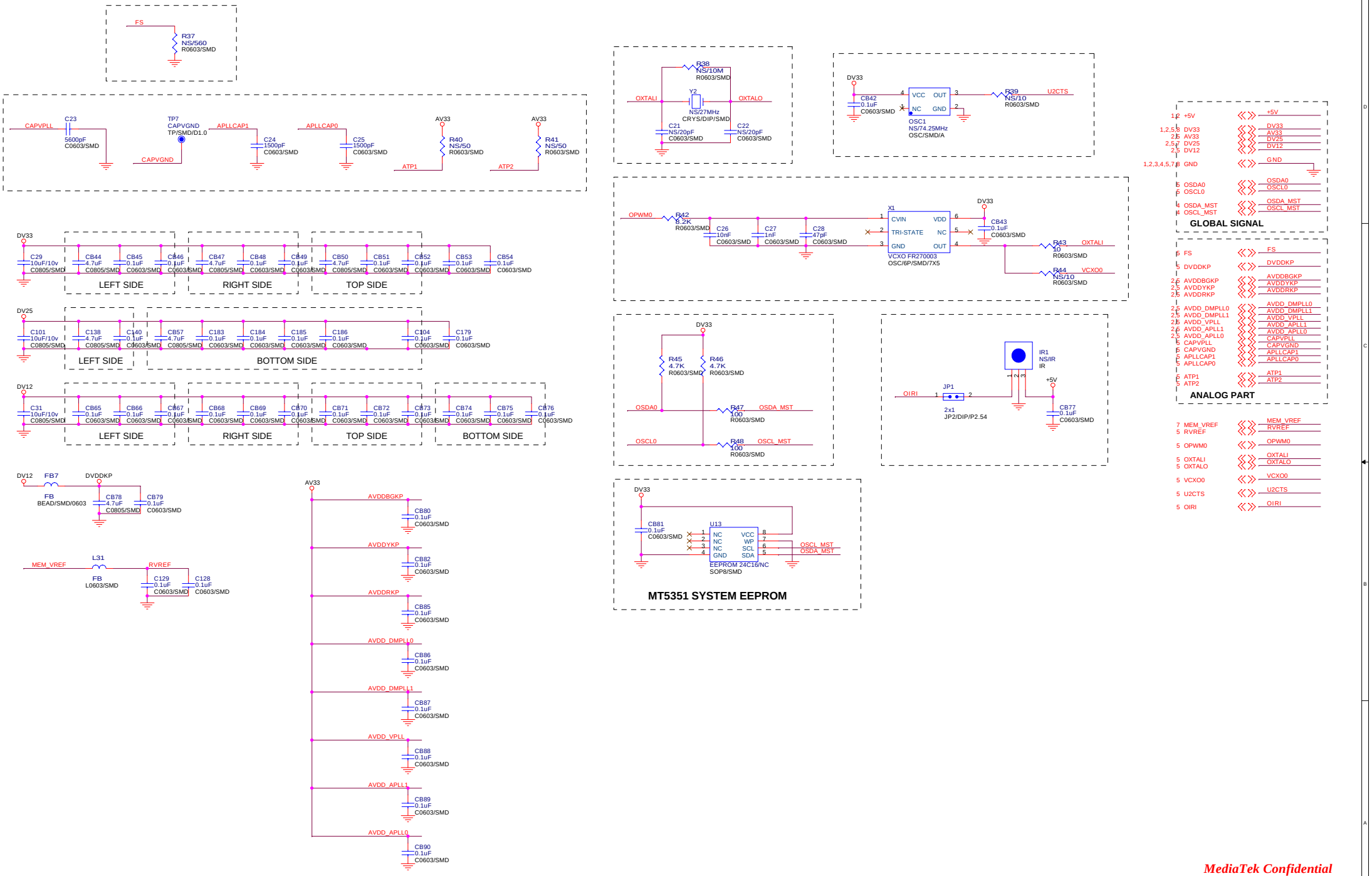

MT5351
GLOBAL SIGNAL
TS INPUT
DDR MEMORY
FLASH INTERFACE
AUDIO INTERFACE
JTAG PORT
UART (RS232)
ANALOG PART
DIGITAL VIDEO OUTPUT
TEST PURPOSE
MT5351
BGA471/SMD
MediaTek Confidential
MT5351 ASIC
MT5351RA-V2
TwinSon Chan
Monday, February 20, 2006
Add by Ada



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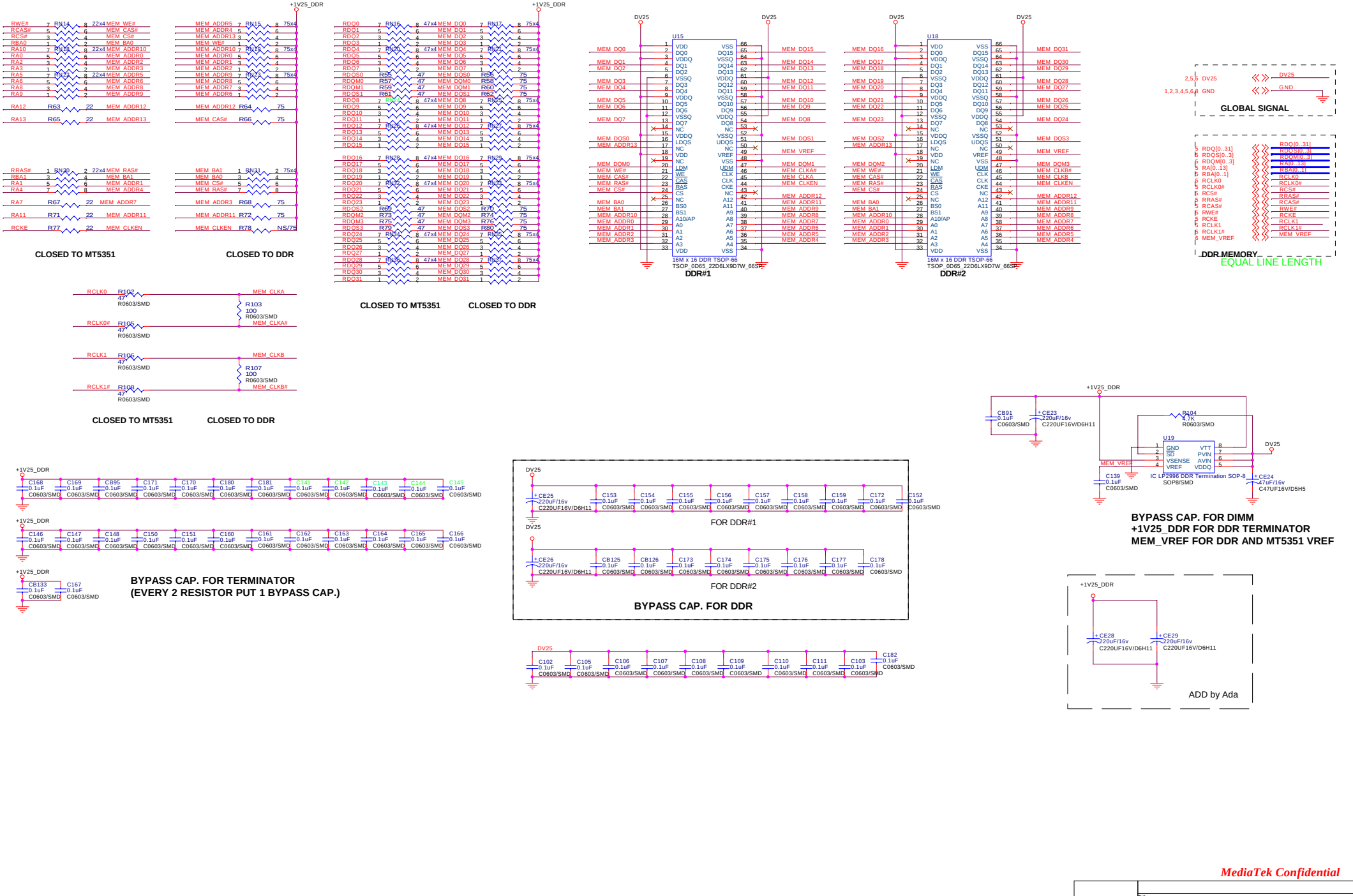
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006	Sheet 6 of 8		



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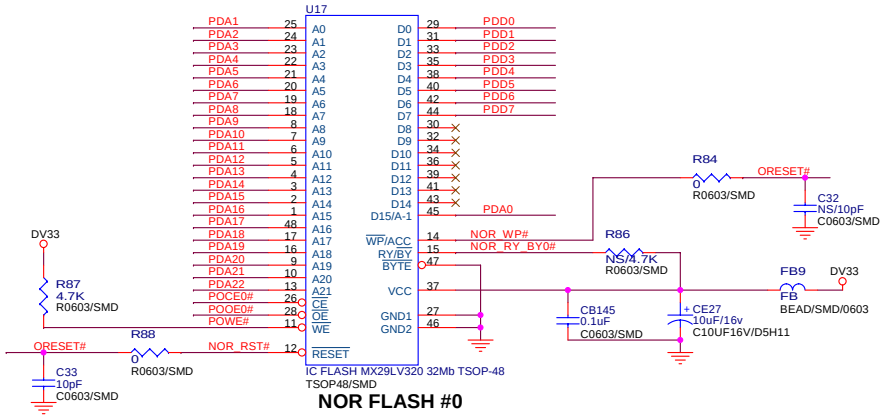
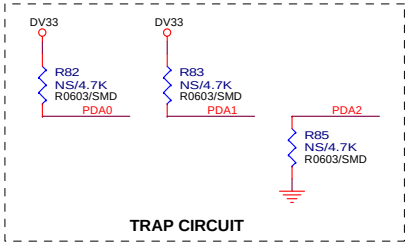
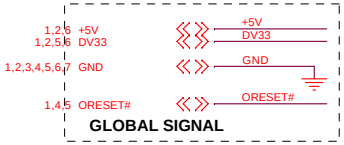
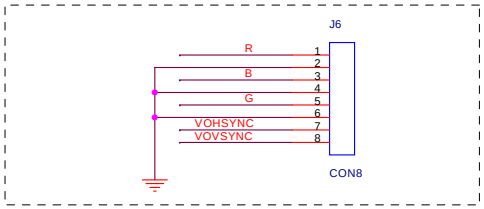
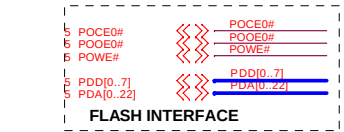
Title: DDR MEMORY			
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
Date: Monday, February 20, 2006		Sheet 7 of 8	

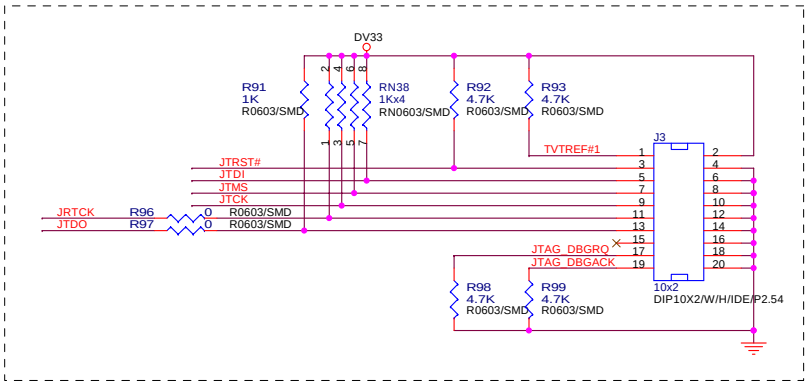

U17
PDA1 PDA2 PDA3 PDA4 PDA5 PDA6 PDA7 PDA8 PDA9 PDA10 PDA11 PDA12 PDA13 PDA14 PDA15 PDA16 PDA17 PDA18 PDA19 PDA20 PDA21 PDA22
POCE0# POOE0# POWE#
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21
CE OE WE RESET
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15/A-1
WP/ACC RY/BY BYTE VCC GND1 GND2
PDD0 PDD1 PDD2 PDD3 PDD4 PDD5 PDD6 PDD7 PDA0
NOR_WP# NOR_RY_BY0#
IC FLASH MX29LV320 32Mb TSOP-48
TSOP48/SMD
DV33
R87 4.7K R0603/SMD
R88 0 R0603/SMD
NOR_RST#
ORESET#
C33 10pF C0603/SMD
R84 0 R0603/SMD
ORESET#
C32 NS/10pF C0603/SMD
R86 NS/4.7K R0603/SMD
CB145 0.1uF C0603/SMD
CE27 10uF/16v C10UF16V/D5H11
FB9 FB BEAD/SMD/0603
DV33
NOR FLASH #0

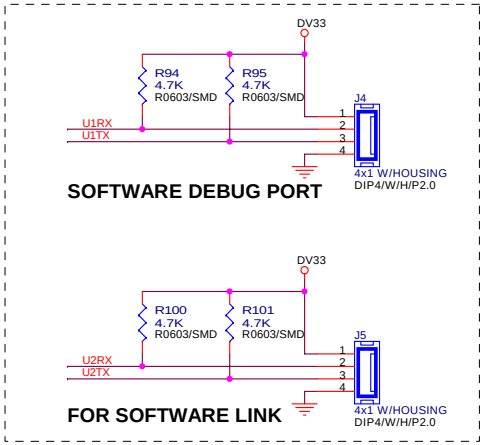


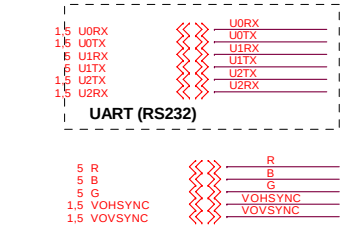


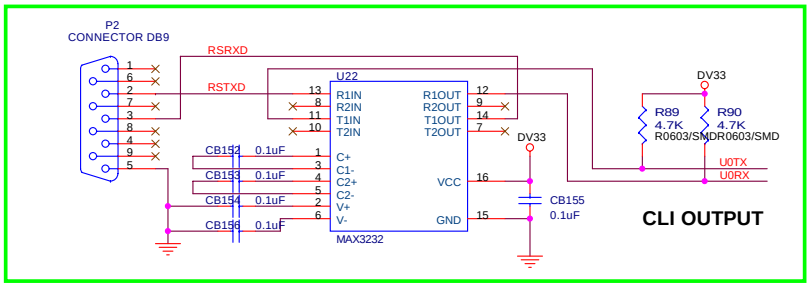


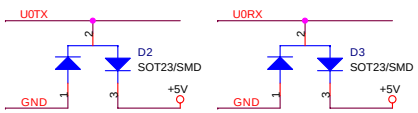












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Title: NOR FLASH / JTAG / UART			
Size: Custom	Document Number: MT5351RA-V2	TwinSon Chan	Rev: 1
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Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 5 pcs PCB including 3 pcs Extension PCB, 1 pcs Timming controller board and 1 pcs Back Light board in the Module.

SET

There are 6 pcs PCBs including 1 pcs ATV Tuner board, 1 pcs keypad board, 1 pcs Remote Control Receiver board, 2 pcs L/R Speakers and 1 pcs Main(Video)board, 1 pcs ATSC board in the SET.

PCB funtion

1. Power :

   (1). Input voltage: AC 120V, 60Hz.

   (2). To provide power for PCBs.

2. Main board : To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI/HDMI signals and D-SUB signals to digital ones and to transmit to Control board.

3. Control board : Dealing with the digital signal for output to panel.

4. Extension board : Output addressing signals.

5. ATV Tuner Board : To convert TV RF signal to video and SIF audio signal to Main board.

6. ATSC Board : Receiver and converter ATSC TV signal to transmit to main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN : a. Lacking color, Bad color scale.
   b. No voice. (Make sure status: Mute / Internal, External speaker)
   c. No picture but with signals output, OSD and back light.
   d. Abnormal noise on screen.
3. POWER : NO picture, no power output.
4. Back Light : a. No picture.
   b. Flash on screen.
   c. Darker picture with signals.
5. ATV Tuner : a. No ATV Noise
   b. No ATV signals
6. ATSC: a No ATSC TV signal

Main IC Specifications

- M13S128168A (ESMT)
  2M x 16 Bit x 4 Banks Double Data Rate SDRAW

- MT5111CE
  Single-Chip HDTV/CATV Demodulator

- MT5351
  MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, MPEG1,2, MP3, AC3 audio decoder, HDTV encoder. MT5351 is powered by ARM 926EJ with 16K I-Cache and 16K D-Cache. It can support 64Mb to 1Gb DDR DRAM devices with configurable 32/64 bit data bus interface.

- MT8202
  MT8202G is a highly integrated Single-Chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals.

- MT8293
  HDMI PanelLink Cinema Receiver

- R2S15102NP
  Digital Power Amplifier R2S15102NP

- WM8776
  24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

MT5111CE
Single-Chip HDTV/CATV Demodulator

Key Features

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -5 to +47*us* range for terrestrial HDTV reception
- On-chip 10-bit ADC for HDTV/CATV demodulator
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- On-chip PLL clock generation
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ±1MHz for ATSC and ±250kHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface
- Controlled by I^2C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-LQFP package
- Lead Free

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Functional Block Diagram

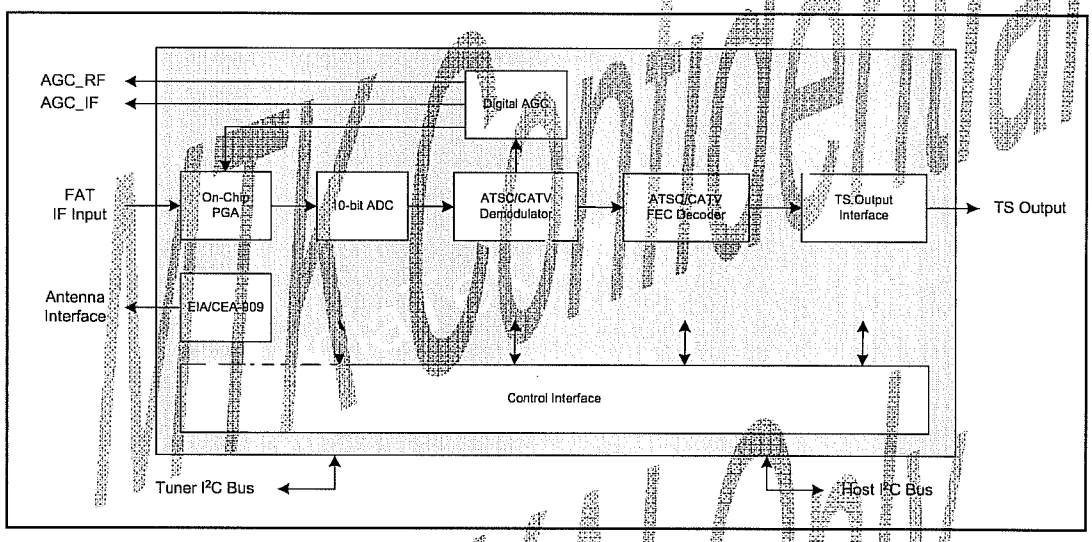

Figure 1: MT5111CE Functional Block Diagram

General Description

MT5111CE is a fully integrated single-chip 8-VSB and 64/256-QAM demodulator. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

MT5111CE includes a 10-bit A/D converter, 8-VSB/QAM demodulator, TCM (Trellis-Coded Modulation) decoder, and Reed-Solomon Forward Error Correction decoder. Moreover, an internal controller handles the acquisition and tracking to ensure the best receiving performance. The internal controller communicates with the external host controller via the I2C-compatible interface, and also provides direct control to the RF tuner via the second I2C-compatible

interface.

MT5111CE accepts either the direct IF signals centered at 44MHz or 43.75MHz, or the low IF signals centered at 5.38MHz. The center frequency of the incoming IF signal can also be programmed to other frequencies for various applications. An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak. The IF signal is first sampled by a 10-bit A/D converter. Afterward, the digitized samples are further processed for adjacent channel interference rejection.

MT5111CE measures the power level of the digitized sequence, and feeds the control voltages back to the RF tuner and the IF amplifier respectively. The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters. The automatic gain control keeps the received power level at a desired level and maximizes the received SNR.

The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer. The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset. All synchronization in MT5111CE are integrated in digital circuits, no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air or over cable networks. The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms, but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation

of TCM and Reed-Solomon decoders. For CATV reception, MT5111CE detects and aligns de-puncturing timing of the received sequence. The timing synchronization is also automatically performed to lock the FEC frames. The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output, TCM decoder, and transport stream packets. The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5111CE also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition, an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111CE is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will try to re-acquire the DTV signal automatically.

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Pin Out

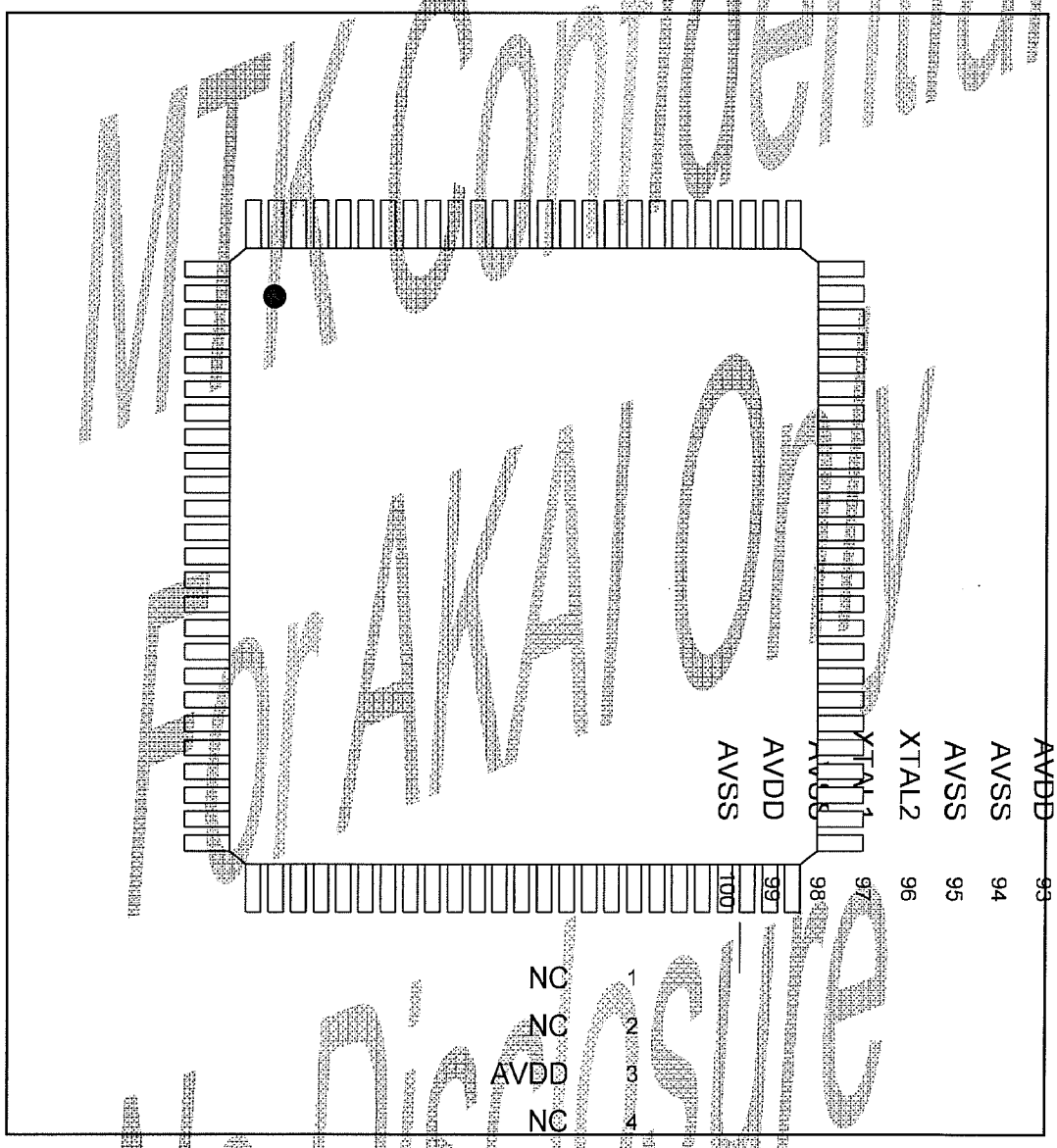

Figure 2: MT5111CE Pin Out

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Pin Description

Signal Name	Pin No	I/O	Description
Transport Stream			
TSDATA[7:0]	22,23,24,25,28, 29,32,33,	O	TS data output
TSSYNC	34	O	TS packet start signal
TSVAL	38	O	TS output valid signal
TSCLK	37	O	TS output clock
TSERR	39	O	TS packet error indicator
Analog Signal			
IN+	82	I	Analog differential IF input
IN-	81	I	
REFTOP	88	O	ADC reference top voltage. Decouple with a capacitor to AVSS
REFBOT	86	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
VCMEXT	87	O	ADC common mode voltage
Antenna Interface			
ANTIF	62	O	CEA-909 Antenna Control Interface
Clock Generation			
XTAL1	97	I	25MHz crystal input
XTAL2	96	I	
Control Signals			
HOST_CLK	47	I	Host processor serial clock input, 5 volt compatible
HOST_DATA	44	I/O	Host processor serial data pin, 5 volt compatible
TUNER_CLK	69	O	Tuner serial clock output, 5 volt compatible
TUNER_DATA	68	I/O	Tuner serial data pin, 5 volt compatible
IF_AGC	72	O	IF AGC output
RF_AGC	73	O	RF AGC output
RESET	48	I	Power reset pin, low active
SA0	66	I	Chip slave address selection pin, tie to VDD3.3 or DGND
SA1	67	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
VDD3.3	17,26,35,42, 52,60,70	P	Digital power supply, tie to 3.3V
VDD1.8	18,30,40,45, 55,64,75	P	Digital power supply, tie to 1.8V
DGND	16,19,27,31, 36,41,43,46,51,56, 61,63,65,71,74	P	Digital ground, tie to digital ground plane
AVDD	3,10,12,80,83,91, 92,93,99	P	Analog power supply, tie to 3.3V
AVSS	7,11,79,85,89,94, 95,98,100		Analog ground, tie to analog ground plane
ADVDD3.3	15,76	P	Digital power supply for analog component, tie to 3.3V
AVDD1.8	90	P	Digital power supply for analog component, tie to 1.8V
Others			
NC	1,2,4,5,6,8,9,13,14, 20,21,49,50,53,54, 57,58,59,77,78,84		Not Connected

Table 1: Pin Description

Electrical Characteristic

Recommended Operating Condition

Symbol	Description	Min	Typical	Max	Unit
Tj	Chip Junction Temperature	-	-	125	°C
VDD1.8	1.8V Digital Core Power Supply Voltage	1.62	1.8	1.98	Volt
AVDD	3.3V Analog Power Supply Voltage	3.15	3.3	3.45	Volt
VDD3.3	3.3V Digital IO Power Supply Voltage	3	3.3	3.6	Volt
AVDD1.8	1.8V Analog Power Supply Voltage	1.7	1.8	1.9	Volt
VIH	Digital Input High Voltage	3	3.3	3.6	Volt
VIL	Digital Input Low Voltage	-	0	-	Volt

Table 2: Recommend Operating Condition

Typical Current and Power Dissipation (ASTC Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	350	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	16	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	630	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	52.8	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	917.4	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 3: Typical Current and Power Dissipation (ATSC Mode)

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Typical Current and Power Dissipation (QAM Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	175	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	19	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	315	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	62.7	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	612.3	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 4: Typical Current and Power Dissipation (QAM Mode)

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MEDIATEK

MT8293

Specifications are subject to change without notice

HDMI PanelLink Cinema Receiver

MT8293 is a low-cost, fully HDMI-compliant receiver that fits directly into home theater products such as LCD TVs, plasma TVs and HDTVs. The receiver is capable of supporting bandwidths up to 165MHz and video resolutions up to 1080p and UXGA. The MT8293 supports the DVD-Audio standard, including 7.1- surround audio at 96kHz and stereo audio at 192kHz.

The built-in High-bandwidth Digital Content Protection (HDCP) decryption engine secures the digital link for transmission of valuable high-definition video and audio.Built-in HDCP self-test engine simplifies manufacturing testing.

FEATHRES

- Industry-Standard
  - HDMI 1.1
  - DVI 1.0
  - EIA/CEA-861B
  - HDCP 1.1
- Digital Video Output
  - Integrated PanelLink Core
  - Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/UXGA) resolution up to 165MHz (using dual edge to transmit video data for pixel clock over 112MHz)
  - Flexible digital video interface
    - 24-bit RGB/YCbCr 4:4:4
    - 16-bit YCbCr 4:2:2
    - 8-bit YCbCr 4:2:2 (ITU-R BT.656)
  - Integrated RGB <-> YCbCr color space conversion (both 601 and 709)
  - 4:2:2 <-> 4:4:4 converter
  - Integrated Deinterlacer for 480i/576i (SDTV only)
  - Integrated Down-Scaler (with CEN)
- Digital Audio Output
  - Industry-standard S/PDIF and 3-wire output
  - Supports high-end audio including DVD-Audio
    - 2-ch. 32-192kHz or
    - 8-ch. 32-96kHz
  - Programmable 3-wire output supports numerous low-cost I2S audio DACs
  - Supports IEC60958 2-channel PCM
  - Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS, etc.)
- Content Protection
  - Integrated HDCP cipher engine
  - External EEPROM for encrypt HDCP keys
  - Built-in HDCP self-test
  - Decrypts both video and audio
- System Operation
  - Register-programmable via slave I2C interface
  - Auto video mode
  - Auto audio mode
  - Flexible interrupt registers with interrupt pin
- Power Management
  - 1.8V core provides low-power operation
  - Flexible power-down modes
- Outline
  - 128-pin QFP package

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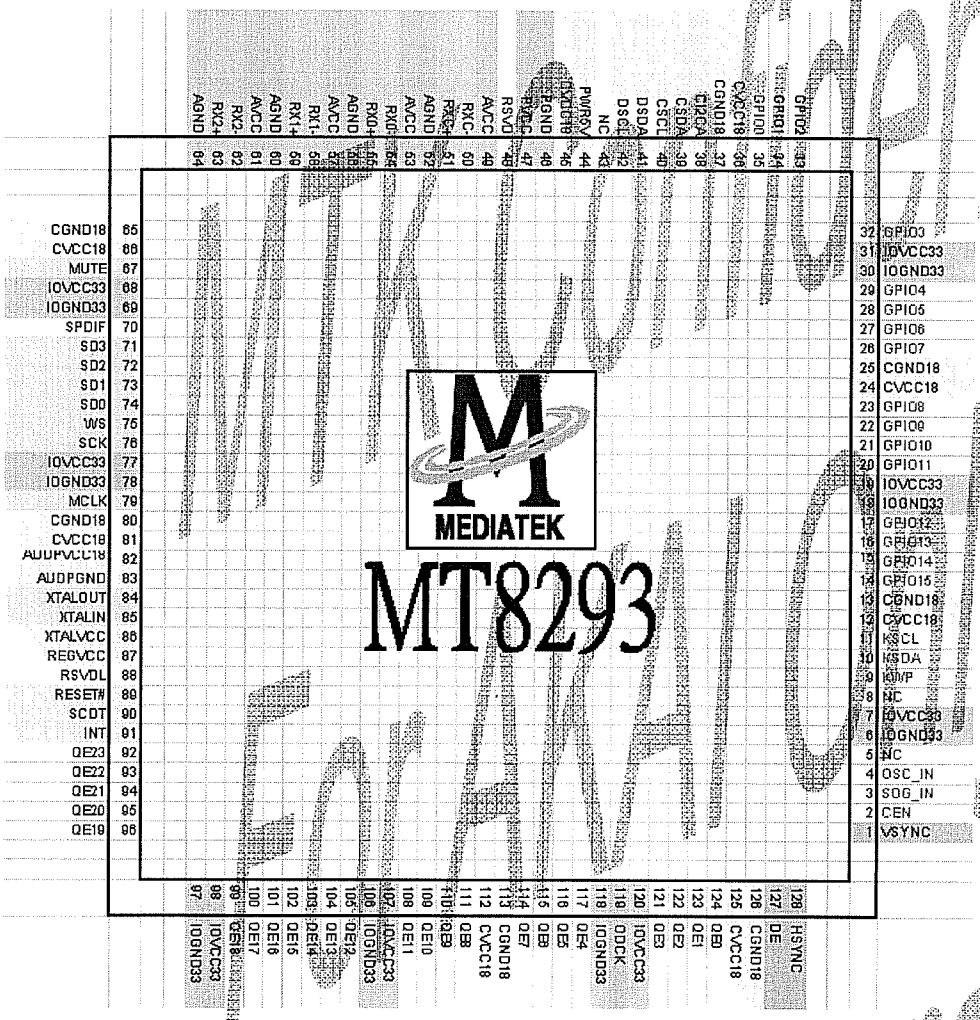

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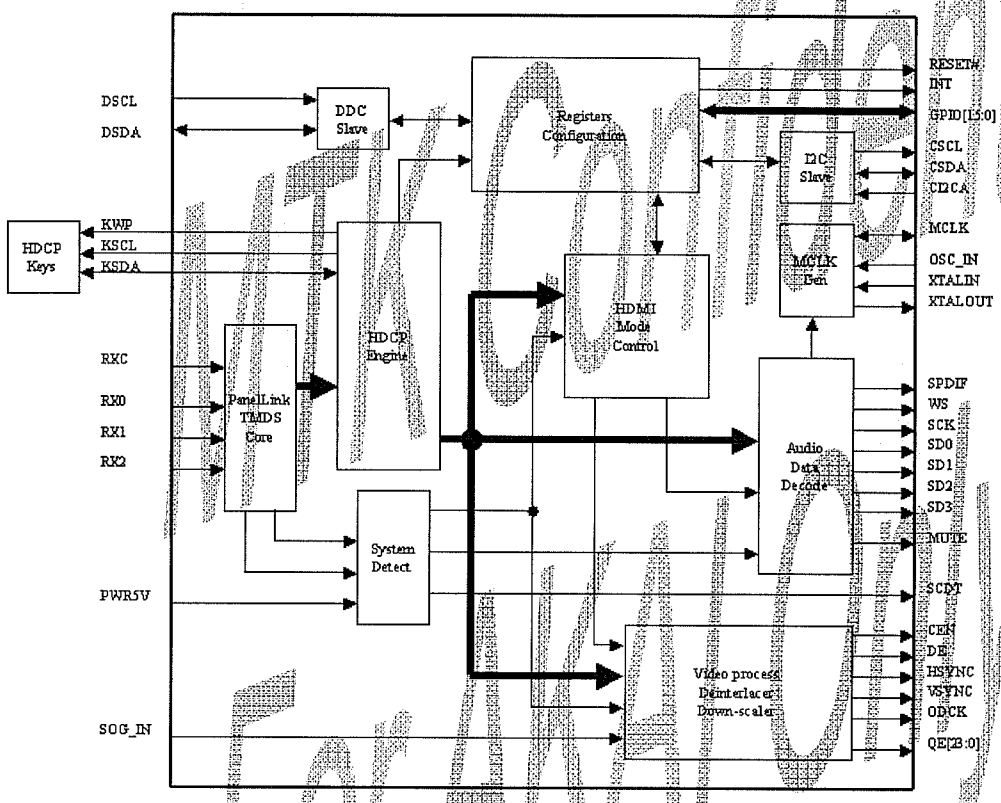

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Item	Symbol	Pin #	Type	Description
DIGITAL				
Power/Ground (45)				
1	CVCC18	12,24,36,45,66,81,112,125	I	Digital Logic 1.8V power
2	CGND18	13,25,37,65,80,113,126	I	Digital Logic ground
3	IOVCC33	7,19,31,68,77,98,107,120	I	Input/Output Pin 3.3V power
4	IOGND33	6,18,30,69,78,97,106,118	I	Input/Output Pin ground
5	AVCC	49,53,57,61	I	TMDS Analog 3.3V power
6	AGND	52,56,60,64	I	TMDS Analog ground
7	PVCC	47	I	TMDS PLL 3.3V power
8	PGND	46	I	TMDS PLL ground
9	AUDPVCC18	82	I	ACR PLL 1.8V power
10	AUDPGND	83	I	ACR PLL ground
11	XTALVCC	86	I	ACR PLL crystal input 3.3V power
12	REGVCC	87	I	ACR PLL regulator 3.3V power
Configuration/Programming (20)				
1	INT	91	O	Interrupt output
2	RESET#	89	I	Reset Pin. Active low
3	DSCL	42	I	DDC I2C clock, 5V tolerance
4	DSDA	41	I/O	DDC I2C data, 5V tolerance
5	CSCL	40	I	Configuration I2C clock
6	CSDA	39	I/O	Configuration I2C data
7	KSCL	11	O	KEYS EEPROM I2C clock
8	KSDA	10	I/O	KEYS EEPROM I2C data
9	KWP	9	O	KEYS EEPROM write protect
10	SCDT	90	O	Indicates active video at HDMI input port
11	CISCA	38	I	I2C device address select

Item	Symbol	Pin #	Type	Description
12	PWR5V	44	I	TMDS port transmitter detect (hot plug), 5V tolerance
13	RSVDL	88	I	Must be tied low
14	RSVD	48	O	
15	NC	43	-	No connect
16	NC	8,5	-	No connect
17	OSC_IN	4	I	Oscillator input, External in
18	SOG_IN	3	I	SOG input, External AD in
19	CEN	2	O	Clock enable, for 8202 CEN input
Digital Audio Interface (9)				
1	MCLK	79	I/O	Audio master clock input reference
2	SCK	76	O	I2S serial clock output
3	WS	75	O	I2S word select output
4	SD0	74	O	I2S serial data output
5	SD1	73	O	I2S serial data output
6	SD2	72	O	I2S serial data output
7	SD3	71	O	I2S serial data output
8	SPDIF	70	O	S/PDIF audio output
9	MUTE	67	O	Mute audio output
GPIO Interface (16)				
1	GPIO0	35	I/O	GPIO
2	GPIO1	34	I/O	GPIO
3	GPIO2	33	I/O	GPIO

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Item	Symbol	Pin #	Type	Description
4	GPIO3	32	I/O	GPIO
5	GPIO4	29	I/O	GPIO
6	GPIO5	28	I/O	GPIO
7	GPIO6	27	I/O	GPIO
8	GPIO7	26	I/O	GPIO
9	GPIO8	23	I/O	GPIO
10	GPIO9	22	I/O	GPIO
11	GPIO10	21	I/O	GPIO
12	GPIO11	20	I/O	GPIO
13	GPIO12	17	I/O	GPIO
14	GPIO13	16	I/O	GPIO
15	GPIO14	15	I/O	GPIO
16	GPIO15	14	I/O	GPIO
TTL Interface (28)				
1	DE	127	O	Data enable
2	VSYNC	1	O	Vertical sync
3	HSYNC	128	O	Horizontal sync
4	ODCK	119	O	Output data clock
5	QE0	124	O	24-bit Even pixel
6	QE1	123	O	24-bit Even pixel
7	QE2	122	O	24-bit Even pixel

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Item	Symbol	Pin #	Type	Description
8	QE3	121	O	24-bit Even pixel
9	QE4	117	O	24-bit Even pixel
10	QE5	116	O	24-bit Even pixel
11	QE6	115	O	24-bit Even pixel
12	QE7	114	O	24-bit Even pixel
13	QE8	111	O	24-bit Even pixel
14	QE9	110	O	24-bit Even pixel
15	QE10	109	O	24-bit Even pixel
16	QE11	108	O	24-bit Even pixel
17	QE12	105	O	24-bit Even pixel
18	QE13	104	O	24-bit Even pixel
19	QE14	103	O	24-bit Even pixel
20	QE15	102	O	24-bit Even pixel
21	QE16	101	O	24-bit Even pixel
22	QE17	100	O	24-bit Even pixel
23	QE18	99	O	24-bit Even pixel
24	QE19	96	O	24-bit Even pixel
25	QE20	95	O	24-bit Even pixel
26	QE21	9	O	24-bit Even pixel
27	QE22	93	O	24-bit Even pixel
28	QE23	92	O	24-bit Even pixel

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Item	Symbol	Pin #	Type	Description
ANALOG (8)				
Differential signal				
1	RXC+	51	I	TMDS input clock pair
1	RXC-	50	I	TMDS input clock pair
1	RX0	55	I	TMDS input data pair
1	RX0	54	I	TMDS input data pair
1	RX1	59	I	TMDS input data pair
1	RX1	58	I	TMDS input data pair
1	RX2	63	I	TMDS input data pair
1	RX2	62	I	TMDS input data pair
PLL group(2)				
68	XTALIN	85	I	Crystal input PAD
69	XTALOUT	84	O	Crystal output PAD

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MEDIATEK

MT8202

HDTV-Ready LCD TV Chip

Specifications are subject to change without notice

MT8202 is a highly integrated single chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals. Embedded HDTV/VGA decoders let the high bandwidth input signals perfectly reproduced. 24/16/8 bits digital port may accept all kinds of external digital input video source. New 2nd generation advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive one with overlay of a 2D Graphic processor. Advanced full function color processing with fully 10-bit path provides high quality video contents. Independent two Flexible scalers provide wide adoption to various LCD panels for two of different video sources at the same time. Its on-chip audio processor decodes analog signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8202 is a cost-effective and high performance HDTV-ready solution to LCD TV manufactures.

FEATURES

- Video Input
  - Support fully programmable 8 Composite/SV input pins
  - Support 2 Component inputs with SDTV format & HDTV 480p/720p/1080i format
  - Support 1 VGA input up to SXGA (1280x1024x75Hz) including SOG signals
  - Support DVI 24-bit RGB digital input
  - Support CCIR-656/601 digital input
- TV decoder
  - Full 10-bit data path to enhance the video resolution and reduce digital truncation errors
  - Support PAL (B,G,D,H,M,N,I,Nc), PAL(Nc), PAL, NTSC, NTSC-4.43, SECAM
  - Automatic Luma/Chroma gain control
  - Automatic TV standard detection
  - 2nd generation NTSC/PAL Motion Adaptive 3D comb filter with huge improvement
  - Motion Adaptive 3D Noise Reduction
  - VBI decoder for Closed-Caption/XDS/ Teletext/WSS/VPS
  - High speed advanced Teletext/Closed-Caption drawing engine directly on OSD plane
  - Macrovision detection
  - Adjustable horizontal delay for combination of SCART Composite/RGB input
- Video Processor
  - Fully 10-bit processing to enhance the video quality
  - Advanced flesh tone and color processing
  - Gamma/anti-Gamma correction
  - Advanced Color Transient Improvement (CTI)
  - 2D Peaking
  - Advanced horizontal/vertical sharpness
  - Saturation/hue adjustment
  - Brightness and contrast adjustment
  - Black level extender
  - White peak level limiter
  - Adaptive Luma/Chroma management
  - Automatic detect film or video source
  - 3:2/2:2 pull down source detection
  - 2nd generation Advanced Motion adaptive de-interlacing
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
  - Advanced linear and non-linear Panorama scaling
  - Programmable Zoom viewer
  - Progressive scan output
  - Picture-in-Picture (PIP)
  - Picture-Out-Picture (POP)
  - Advanced dithering processing for LCD display with 6/8/10 bit output
  - Frame rate conversion, 50Hz to 75Hz
- Audio DSP
  - Support BTSC/EIAJ/A2/NICAM decode
  - Stereo demodulation, SAP demodulation

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- Noise reduction
- Mode selection (Main/SAP/Stereo)
- Pink noise and white noise generator
- Equalizer
- Sub-woofer/Bass enhancement
- Noise auto mute
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support Reverberation

Audio Input/Output

- Decode audio AF from Tuner
- 2 channel audio L/R digital line in
- 7.1-channel slave digital line in
- Including full 7.1-channels digital output, 2-channel bypass and 2-channel headphone output
- Embedded 3 internal DAC output

DRAM Controller

- Supports up to 32M-byte SDR/DDR DRAM
- Supports 2x16 bit SDR/DDR bus interfaces
- Build in a DRAM interface programmable clock to optimize the DRAM performance
- Programmable DRAM access cycle and refresh cycle timings
- Support 3.3/2.5-Volt SDR/DDR Interface

Video Output

- TV pattern generator for testing
- Interlaced 50Hz to 120Hz
- Support up to 1366 horizontal points
- 6/8/10-bit single channel or 6/8/10-bit dual channel LVDS output
- Support video output mirror and upside down

2D-Graphic/3 OSD processor

- Embedded Two backend RGB domain OSD planes and one YUV domain OSD
- Support Text/Bitmap decoder
- Support line/rectangle/gradient fill
- Support bitblt
- Support color Key function
- Support Clip Mask
- Support Alpha blending with video output
- 65535/256/16/4/2-color bitmap format OSD,
- Automatic vertical scrolling of OSD image
- Support OSD mirror and upside down

Host Micro controller

- Turbo 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 2048-bytes on-chip RAM
- Up to 4M bytes FLASH-programming interface
- Supports 5/3.3-Volt FLASH interface
- Supports power-down mode
- Supports additional serial port
- IR control serial input
- Support 2 RS232 interface for external source communication
- Support 2 PWM output
- Support DDC2Bi/DDC2B/DDC1/DDCCI
- Programmable GPIO setting for complex external device control

Outline

- 388-pin BGA package
- Lead Free
- 3.3/2.5/1.8-Volt operating voltages
- 0.18um process

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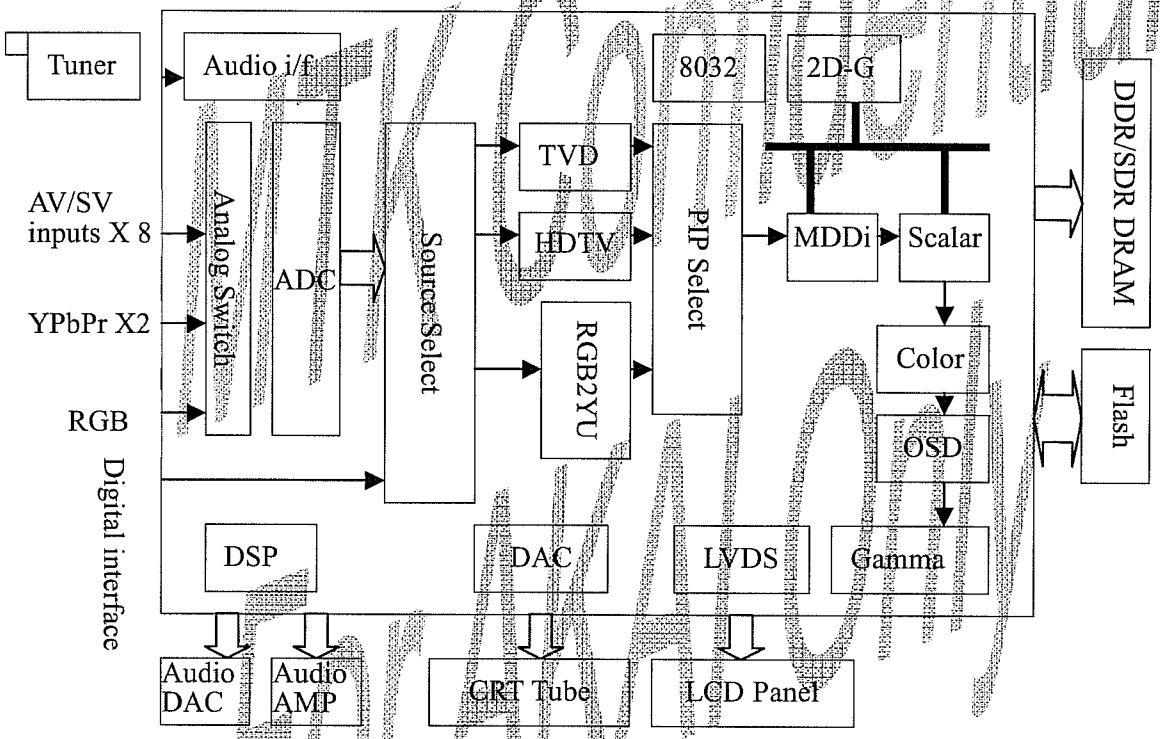
BLOCK DIGRAM



Analog Switch

Analog switches are built in MT8202 to connect to 17 input signals and there is need to add external components to add analog video multiplexes on board.

There are 9 high-speed differential input pairs for 3 sets of YPRPB/VGA input signals.

The 8 Composite/S signal input pins can be fully programmed to connect to any AV/SV inputs.

ADC/ Source Select

The video ADC sample analog input signals. After ADC, all signal processing is digital domain. The source select multiplex all inputs from digital and analog video ports and route them into data path.

Audio Interface

Audio interface accept analog audio signal from Tuner, e.g. AF. It also includes preprocessing circuit to filter the noisy audio signals. Audio decoder will decode the BTSC or NICAM, and output best sound with enhanced 3D surround post-processing.

Embedded 7.1 channel digital audio input (slave) and 2 channels (master) digital audio inputs.

Embedded 3 high performance audio DACs.

DSP

DSP handle audio decoding as well as computing intensive jobs. The downloadable micro code enables fast function convergence for various audio standards in the world.

Advanced DSP engine supports full functions of sound effects.

MDDi/Scaler

MDDi is MTK proprietary de-interlacing technology, 2nd generation MDDi solution provides improved low angle processing and more accurate motion detection for all interlace sources. The techniques reduce jagged edges and broken images. The MDDi engine supports both Main and Sub channel SDTV inputs or one channel 1080i high quality de-interlacing.

Two totally independent scaler support full functions of PIP/POP and frame rate conversion.

With MDDi and high quality scaler, MT8202 guarantee all input format could be translated to output format with best video quality for motion and still pictures.

Color/Gamma

MT8202 includes advanced color management function to allow user to improve video quality with fully flexibility. With contrast/hue/saturation/Gamma/anti-Gamma/flesh tone function, MT8202 deliver the best video quality with vivid color.

Advanced dither function support 6/8/10-bit video output for any kinds of display unit (LCD, PDP, CRT).

8032

On-chip Turbo8032 provide the most cost effective development environment for system house. Well-proven F/W could speed up the system design significantly.

2D-G/OSD

On-chip graphic engine draw bitmap OSD and store them into DRAM. OSD read data from DRAM and display on screen. With 2D-G and OSD. The computing power requirement of μP will be minimized.

One YUV space OSD added to support Main/PIP Teletext/Close-caption functions.

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MEDIATEK

MT5351

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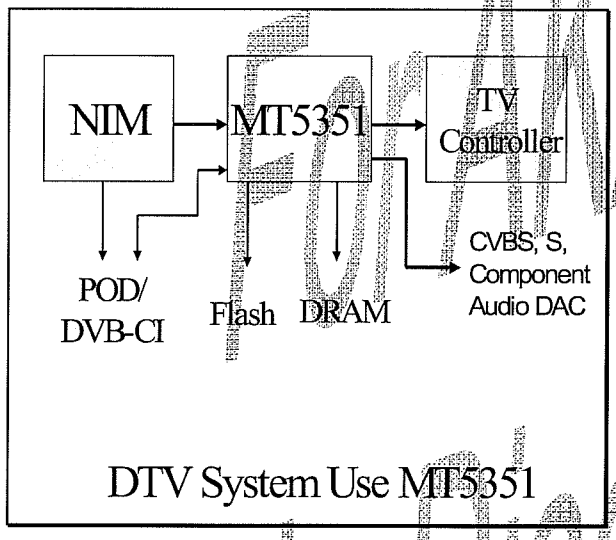
DTV Backend Decoder SOC

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, JPEG decoder, MPEG1,2, MP3, AC3 audio decoder, HD TV encoder. The MT5351 enables consumer electronics manufactures to build high quality, feature-rich DTV, STB or other home entertainment audio/video device.

World-Leading Technology: HW support worldwide major broadcast network and CA standards, include ATSC, DVB, OpenCable, DirectTV, MHP.

Rich Feature for high value product: To enrich the feature of DTV, the MT5351 support 1394-5C component to external DVHS. Dual display, PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality: The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The embedded 4X over-sample video DAC could generate very fine display quality. Also, the audio 3D surround and equalizer provide professional entertainment



DTV System Use MT5351

Key Features:

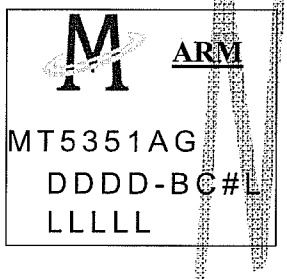
1. Flexible Demuxer
2. Dual HD MPEG2 Video Decoder
3. Dual MPEG1,2, MP3, AC3 Audio decode
4. Dual Display
5. PIP/POP/Quad Mode
6. IEEE1394-5C
7. POD/DVB-CI

Application:

1. DTV
2. Set-top Box
3. DTV Recorder
4. Home Media Center

Order Information:

MT5351AG → one HD decoder
MT5351CG → two HD decoder
All Package are Lead Free



IC Top View:

DDDD: Date Code
#: Subcontractor Code
LLLLL: Lot Number

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General Feature List

- Host CPU
  - ARM 926EJ
  - 16K I-Cache and 16K D-Cache
  - 8K Data TCM and 8K Instruction TCM
  - JTAG ICE interface
  - Watch Dog timers
- Transport Demuxer
  - Support 3 independent transport stream inputs.
  - Support serial / parallel interface for each transport stream input.
  - Support ATSC, DVB, and MPEG2 transport stream inputs.
  - Programmable sync detection.
  - Support DES/3-DES de-scramble
  - 96 PID filter and128 section filters.
  - Support TS recording via IEEE1394 interface
- MPEG2 Decoder
  - Support dual MPEG-2 HD decoder or up to 8 SD decoder
  - Complaint to MP@ML, MP@HL and MPEG-1 video standards
- JPEG Decoder
  - Decode Base-line or progressive JPEG file
- 2D Graphics
  - Support multiple color modes
  - Point, horizontal/vertical line primitive drawing
  - Rectangle fill and gradient fill functions
  - BitBlt with transparent, alpha blending, alpha composition and stretch
  - Font rendering by color expansion
  - Support clip masks
  - YCbCr to RGB color space transfer
- OSD Display
  - 3 linking list OSDs with multiple color mode
  - OSD scaling with arbitrary ratio from 1/2x to 2x
  - Square size, 32x32 or 64x64 pixel, hardware cursor
- Video Processing
  - Advanced Motion adaptive de-interlace on SDTV resolution
  - Support clip
  - 3:2/2:2 pull down source detection
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/15X to 16X
  - Support Edge preserve
  - Support horizontal edge enhancement
  - Support Quad-Picture
- Main Display
  - Mixing two video and three OSD and hardware cursor
  - Contrast/Brightness adjustment
  - Gamma correction
  - Picture-in-Picture (PIP)
  - Picture-Out-Picture (POP)
  - 480i/576i/480p/576p/720p/1080i output
- Auxiliary Display
  - Mixing one video and one OSD
  - 480i/576i output
- TV Encoder
  - Support NTSC M/N, PAL M/N/B/D/G/H/I
  - Macrovision Rev 7.1.L1
  - CGMS/WSS
  - Closed Captioning
  - Six12-bit video DACs for CVBS, S-video or RGB/YPbPr output
- Digital Video Interface
  - Support SAV/EAV
  - Support 8/16 for SD/HD digital video input
  - Support 8/16/24 bits digital output for main display
  - Support 8 bits digital output for aux display
- DRAM Controller
  - Supports 64Mb to 1Gb DDR DRAM devices
  - Configurable 32/64 bit data bus interface
  - Support DDR266, DDR333, DDR400 JEDEC specification compliant SDRAM
- Peripheral Bus Interface
  - Support NOR/NAND flash
  - Support CableCard host control bus
- Audio

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- Support Dolby Digital AC-3 decoding
- MPEG-1 layer I/II, MP3 decoding
- Dolby prologic II
- Main audio output: 5.1ch + 2ch (down mix)
- Auxiliary audio output: 2ch
- Pink noise and white noise generator
- Equalizer
- Bass management
- 3D surround processing include virtual surround
- Audio and video lip synchronization
- Support reverberation
- SPDIF out
- I2S I/F

■ Peripherals

- Three UARTs with Tx and Rx FIFO, two of them have hardware flow control
- Two serial interfaces, one is master only; the other can be set to master mode or slave mode
- Two PWMs
- IR blaster and receiver
- IEEE 1394 link controller
- IDE bus: ATA/ATAPI7 UDMA mode 5, 100 MB/s
- Real-time clock and watchdog controller
- Memory card I/F: MS/MS-Pro, SD, CF, and MMC
- PCMCIA/POD/CI interface

■ IC Outline

- 471 Pin BGA Package
- 3.3V/1.2V dual Voltage

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Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD	Analog supply voltage	-0.5 to 4.6	V
RVDD	DDR supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			
VOL(3.3V)	3.3V output voltage low			0.4	
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissapation		1.5		W
Pdown	Power down mode		2		mW

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DDR ELECTRICAL Characteristics and DC Operating Condiction

Symbol	Parameters	Min	Typ	Max	Unit
RVDD(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

DDR AC Operating Condiction

Symbol	Parameters	Min	Typ	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

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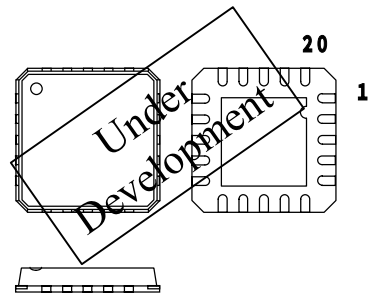
10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V,THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

Fig. 1 Package



20pin QFN
Body : 6 x 6 mm
Lead pitch : 0.8 mm

2.Feature

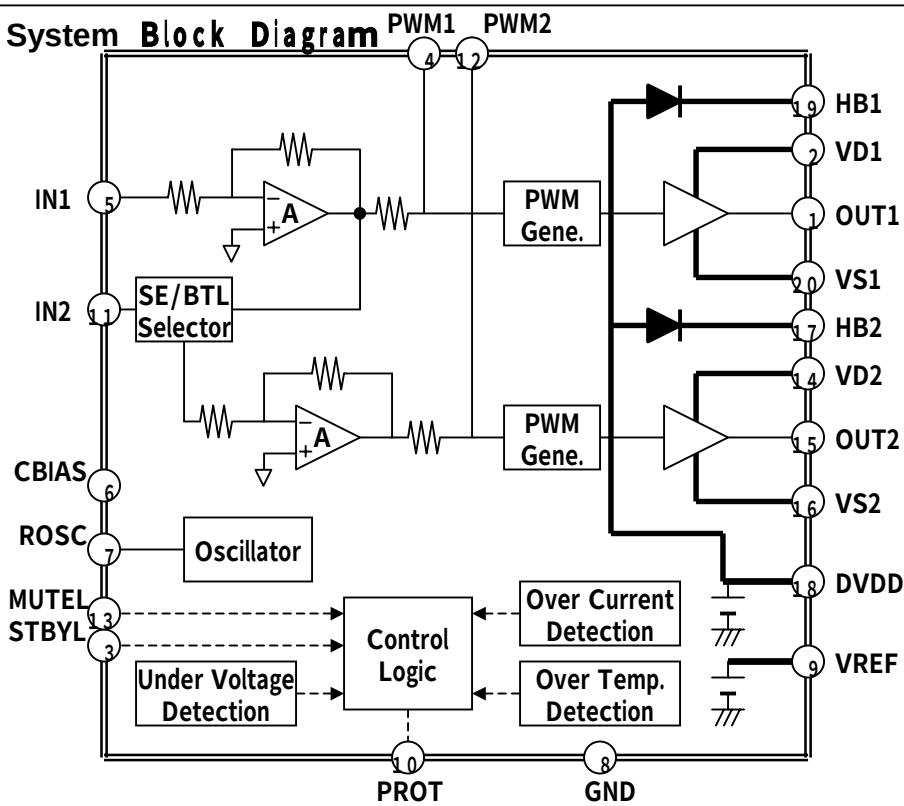
- **High** Output Power(THD=10%)**without external Heat Sink**
  (note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.
  Recommanded Power Condition
  SE operation mode :10Wx2ch(VD=24V) at 8 Ω
  BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω
- The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.
- **Pop sound Less**
- **Built-in protection function**
  (Over Current, Over Temperature and Under Voltage)
- **Built-in Mute and Stand-by function**

3.Operating Condition

- **Recommanded** Power supply voltage : **from 11V to 25V**
- **Recommanded** Speaker Impedance : from 4 to 8Ω

4.Block Diagram

Fig. 2 System Block Diagram



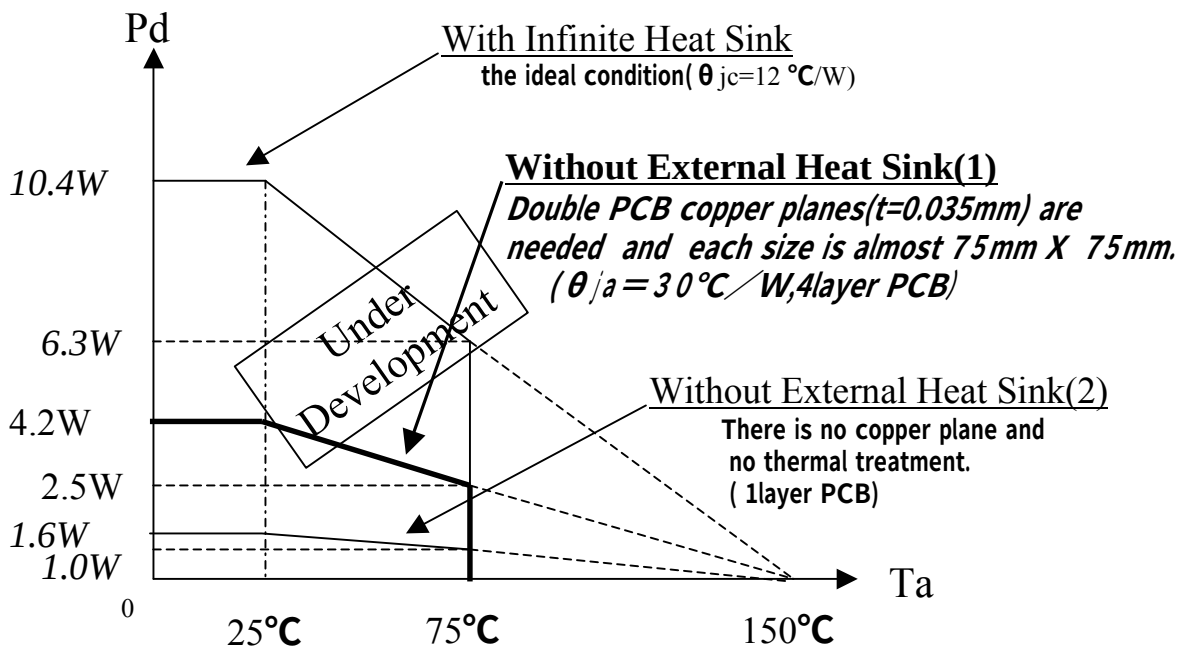
5. Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	**OUT1**	O	Power Output pin #1	
2	**VD1**	—	Power supply pin for power output stage #2	
3	**STBYL**	I	Stand-by control pin. When this is “L”, circuit current is reduced.There is the pull-down resistor:50Kohm(typ.).	
4	**PWM1**	I	PWM input pin #1 (for phase compensation)	
5	**IN1**	I	Analog input #1. The gain is depended on the external resistance .	
6	**CBIAS**	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	**ROSC**	I	Control pin for PWM carrier frequency	
8	**GND**	—	GND pin for analog block	
9	**VREF**	I/O	Capacitor connection pin for analog block reference voltage source	
10	**PROT**	O	Protection Timer pin. At protection mode,the output becomes “L”-level. (The timing capacitor is connected)	
11	**IN2**	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resister, Reversed signal of OUT1 is output to OUT2.
12	**PWM2**	I	PWM input pin#2 (for phase compensation)	
13	**MUTEL**	I	Mute control pin. When this is “L”, it becomes mute status.	
14	**VD2**	—	Power supply pin for power output stage #2	
15	**OUT2**	O	Power Output pin #2	
16	**VS2**	—	Ground pin for power output stage #2	
17	**HB2**	I/O	Capacitor connection pin for bootstrap	
18	**DVDD**	O	Built-in power supply pin for internal digital block.	
19	**HB1**	I/O	Capacitor connection pin for bootstrap #1	
20	**VS1**	—	Ground pin for power output stage #1	

6. Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1、HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
θja	Thermal Resistance	See Fig.3	30	℃/W
Tj	Junction temperature	Maximum Temperature	150	℃
Ta	Operating ambient temperature	Temperature range	-20～75	℃
Tstg	Storage temperature	Temperature range	-40～150	℃

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

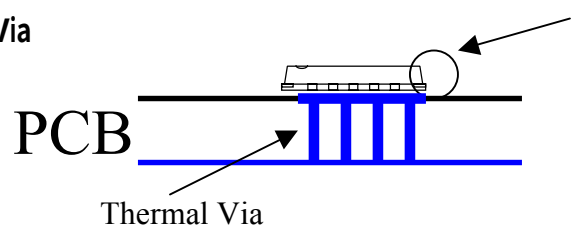


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is directly soldered with the printed-circuit board pattern .

(2)Thermal Via



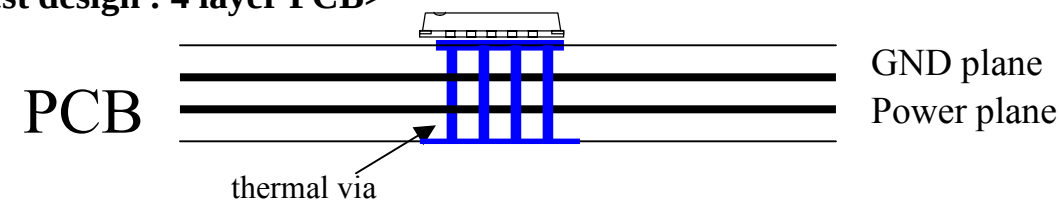
(caution)
There are side expositions of the die pad at corners of the package.
(The die pad is grounded.)

Consideration about the PCB design

The Power dispassion at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at θja=30℃/W.

(1)PCB basic design (copper plane)

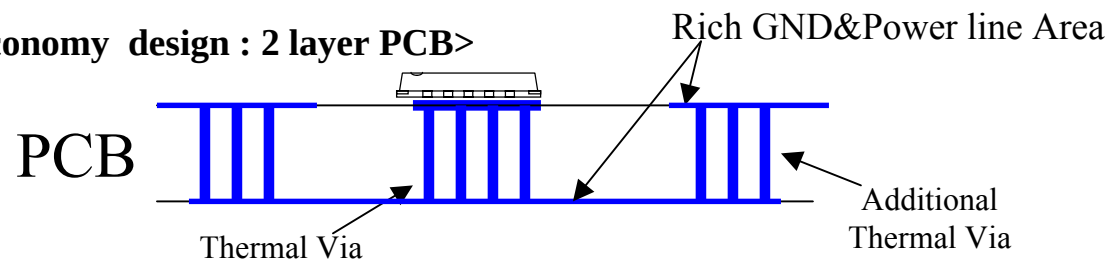
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



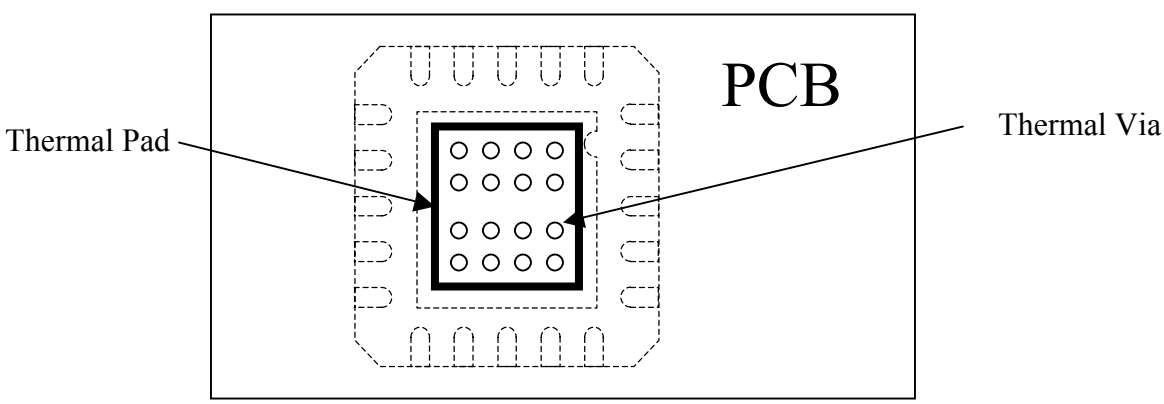
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+α)mm x (75+α) mm

(2)PCB Thermal Pad

The exposed die pad is directly soldered with the printed-circuit board pattern .



7. Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL、MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL、MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33kΩ	300	400	600	kHz

(note) ・STBYL: High level:normal operation Low level:Stand-by
・MUTEL:High level:normal operation Low level:Mute
・The carrier frequency can be changed by the resistance at Pin#.7 .

8. Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	℃
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	℃
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8Ω	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8Ω	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100Hz	TBD	50	-	dB

9. Application Examples

(note)
"R for GND" 's are for the evaluation only and not needed actually.

Fig.4 SE operation mode(10Wx2ch)

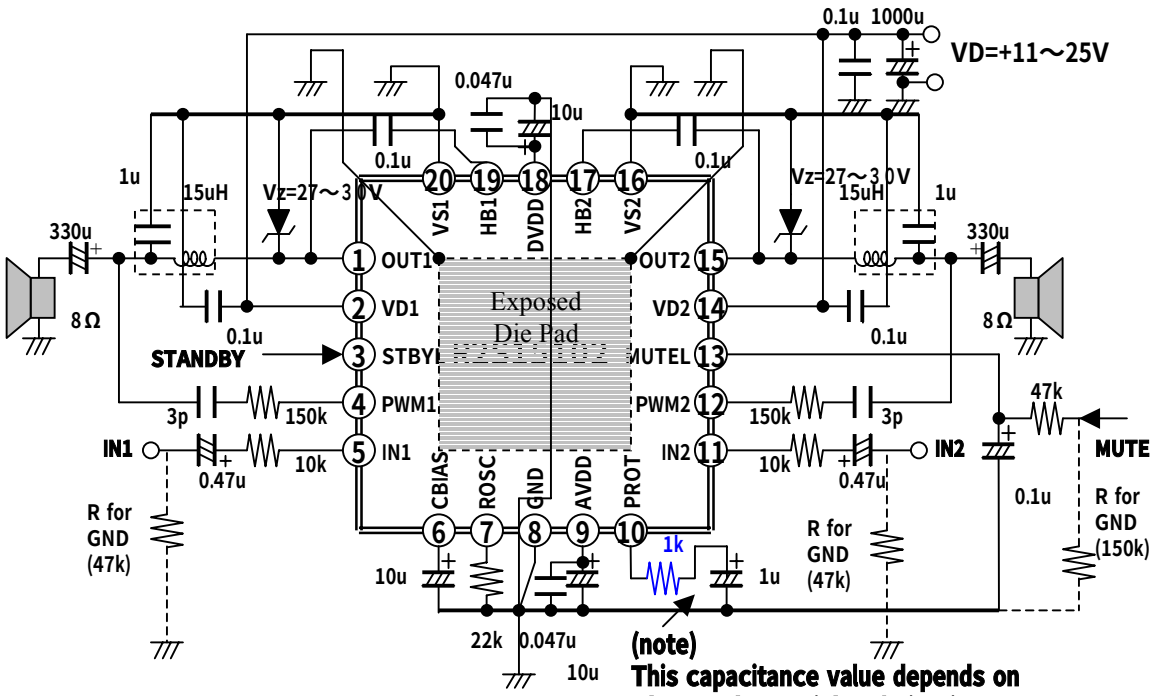


Fig.5 BTL operation mode (20W)

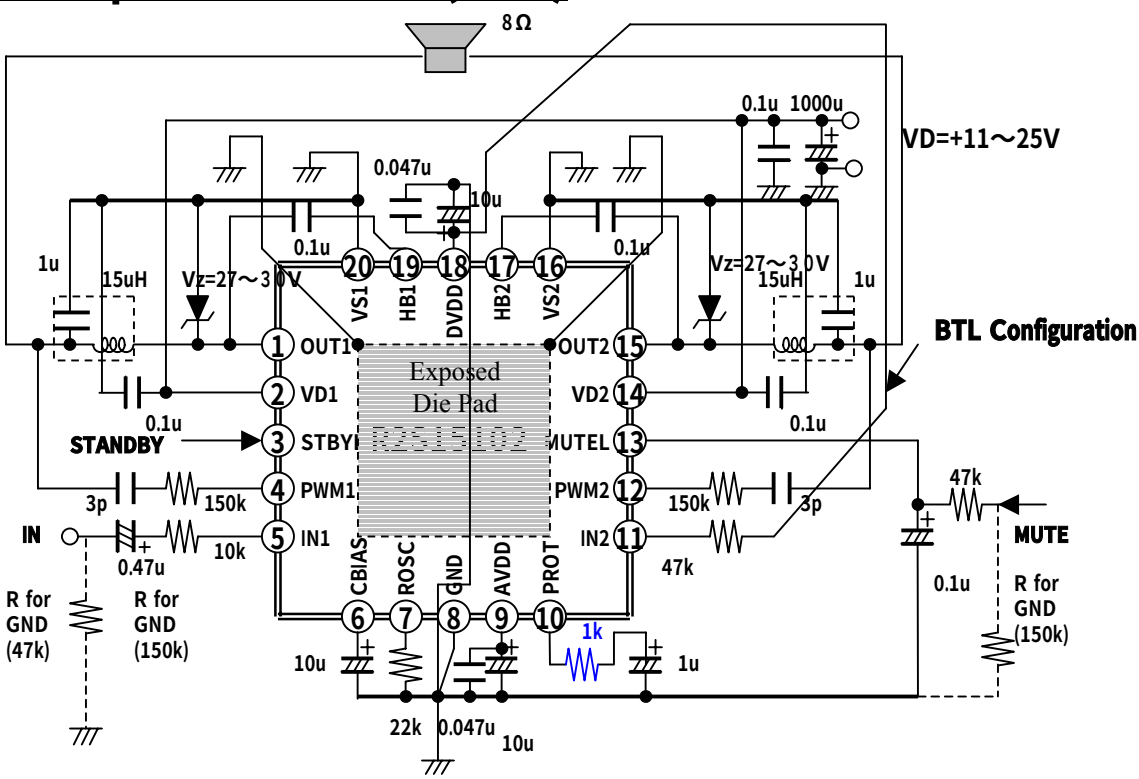


Fig.6 BTL operation mode(20W) with PWM direct input

(note)
"R for GND" 's are for the evaluation only and not needed actually.

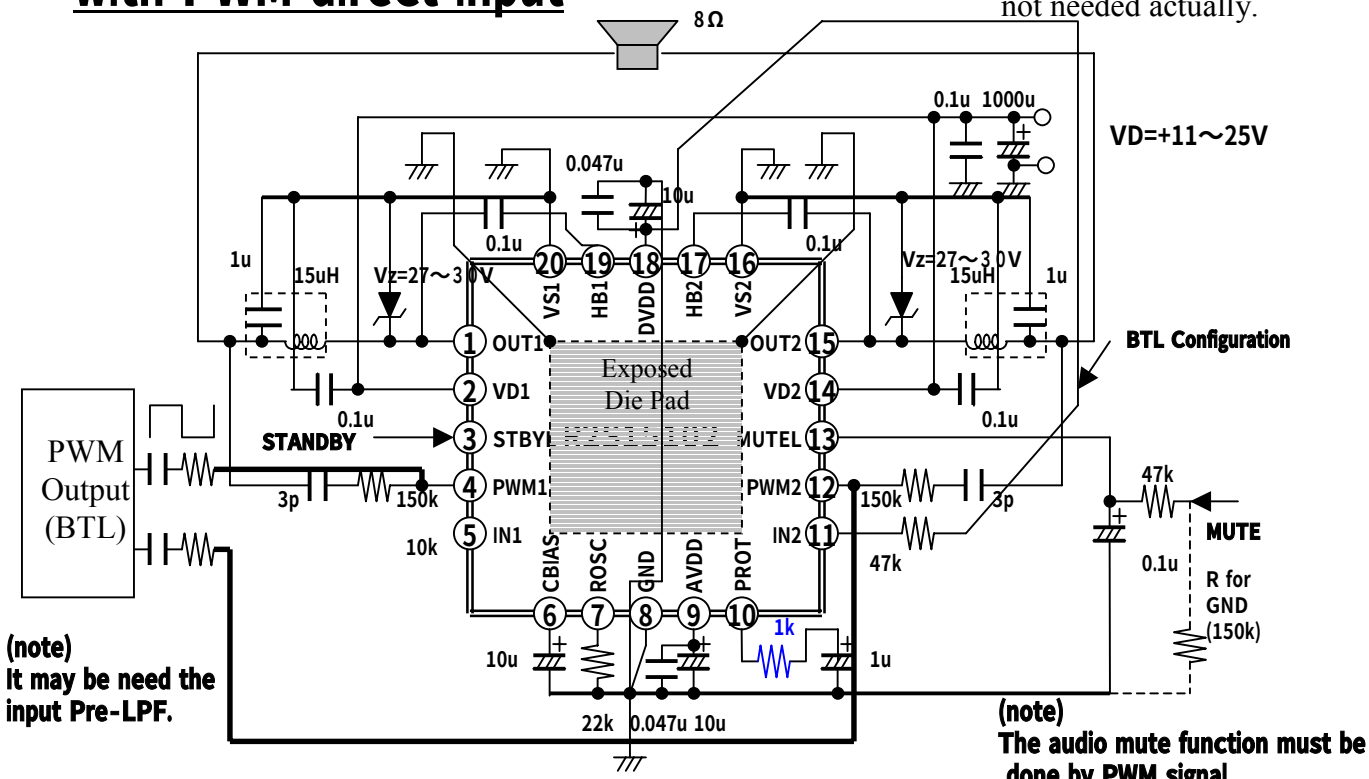
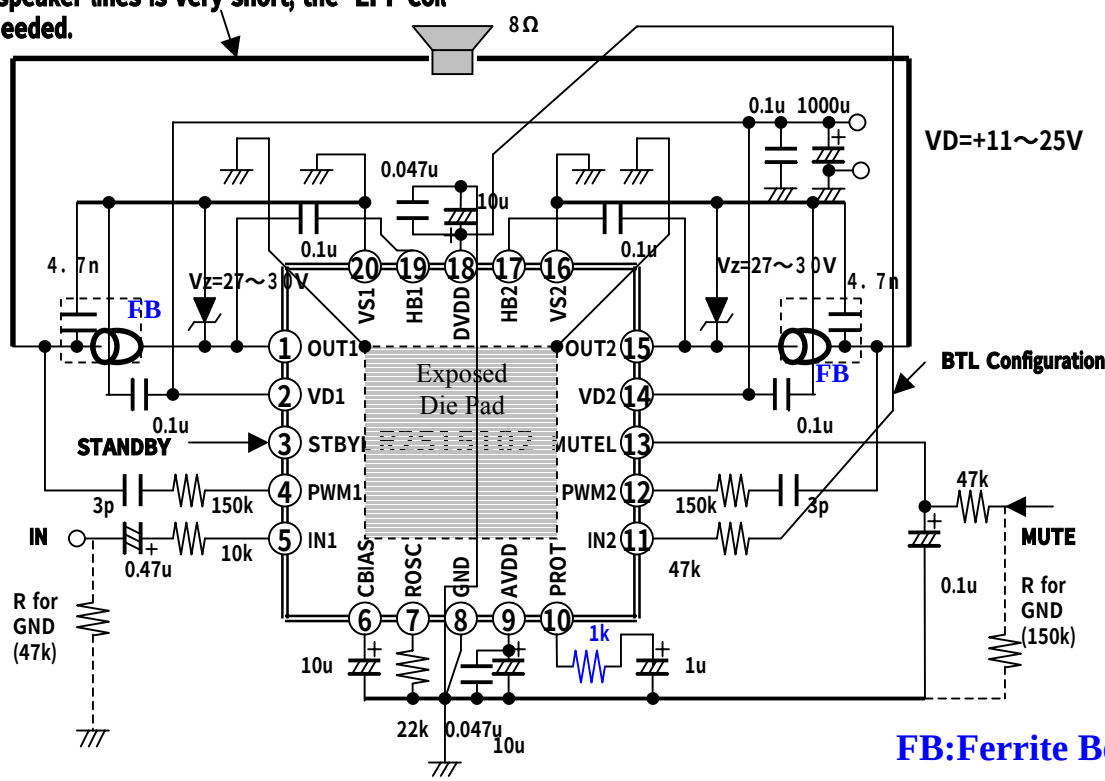


Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



WM8776

24-bit, 192kHz Stereo Codec with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I^2S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

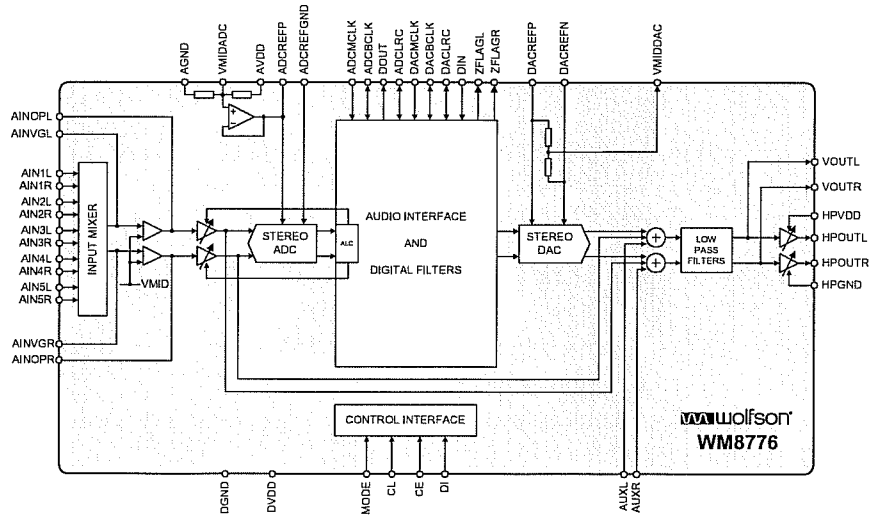
FEATURES

- Audio Performance
  - 108dB SNR ('A' weighted @ 48kHz) DAC
  - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

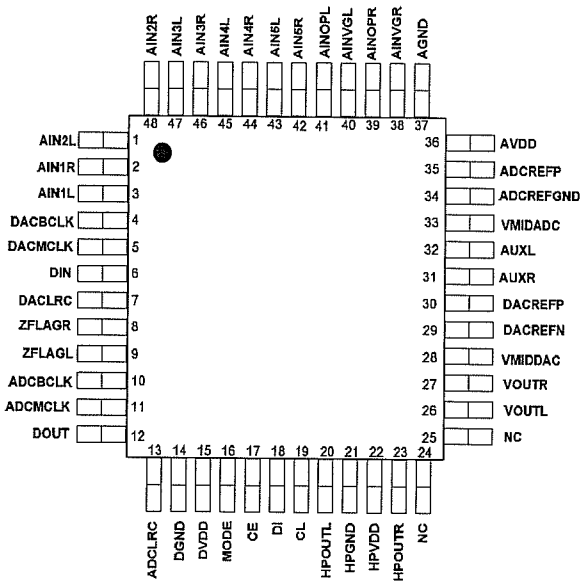
APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8776EFT/V	-25 to +85°C	48-pin TQFP	MSL2	240°C
WM8776EFT/RV	-25 to +85°C	48-pin TQFP (tape and reel)	MSL2	240°C
WM8776SEFT/V	-25 to +85°C	48-pin TQFP (lead free)	MSL2	260°C
WM8776SEFT/RV	-25 to +85°C	48-pin TQFP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
4	DACBCLK	Digital input/output	DAC audio interface bit clock
5	DACMCLK	Digital input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital input/output	DAC left/right word clock
8	ZFLAGR	Open Drain output	DAC Right Zero Flag output (external pull-up resistor required)
9	ZFLAGL	Open Drain output	DAC Left Zero Flag output (external pull-up resistor required)
10	ADCBCLK	Digital input/output	ADC audio interface bit clock
11	ADCMCLK	Digital input	ADC audio interface master clock
12	DOUT	Digital output	ADC data output
13	ADCLRC	Digital input/output	ADC left/right word clock
14	DGND	Supply	Digital negative supply
15	DVDD	Supply	Digital positive supply
16	MODE	Digital input	Control interface mode select (5V tolerant)
17	CE	Digital input	Serial interface Latch signal (5V tolerant)
18	DI	Digital input	Serial interface data (5V tolerant)
19	CL	Digital input	Serial interface clock (5V tolerant)
20	HPOUTL	Analogue Output	Headphone left channel output
21	HPGND	Supply	Headphone negative supply
22	HPVDD	Supply	Headphone positive supply
23	HPOUTR	Analogue Output	Headphone right channel output
24	NC	Not bonded	
25	NC	Not bonded	
26	VOUTL	Analogue output	DAC channel left output
27	VOUTR	Analogue output	DAC channel right output
28	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
29	DACREFN	Analogue input	DAC negative reference input
30	DACREFP	Analogue input	DAC positive reference input
31	AUXR	Analogue input	DAC mixer right channel input
32	AUXL	Analogue input	DAC mixer left channel input
33	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
34	ADCREFGND	Supply	ADC negative supply and substrate connection
35	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
36	AVDD	Supply	Analogue positive supply
37	AGND	Supply	Analogue negative supply and subVstrate connection
38	AINVGR	Analogue Input	Right channel multiplexor virtual ground
39	AINOPR	Analogue Output	Right channel multiplexor output
40	AINVGL	Analogue Input	Left channel multiplexor virtual ground
41	AINOPL	Analogue Output	Left channel multiplexor output
42	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
43	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
44	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
45	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
46	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
47	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
48	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers and pins 16, 17, 18 and 19 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE and MODE)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK and DACBCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}=1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBFs Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, @ fs = 48kHz		108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input		108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Headphone Buffer						
Maximum Output voltage				0.9		Vrms
Max Output Power (Note 4)	P_o	R_L = 32 Ω		25		mW
		R_L = 16 Ω		50		mW
SNR (Note 1,2)		A-weighted	85	92		dB
Headphone analogue Volume Gain Step Size			0.5	1	1.5	dB
Headphone analogue Volume Gain Range		1kHz Input	-73		+6	dB
Headphone analogue Volume Mute Attenuation		1kHz Input, 0dB gain		100		dB
Total Harmonic Distortion +Noise	THD+N	1kHz, R_L = 32Ω @ P_o = 10mW rms		-80 0.01	-60 0.1	dB %
		1kHz, R_L = 32Ω @ P_o = 20mW rms		-77 0.014	-40 1.0	dB %
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz, without supply decoupling		-40		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz		102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		100		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-90	-80	DB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

		1kHz, -3dBFs		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1)			90	100		dB
THD		1kHz, 0dB		-90		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. Harmonic distortion on the headphone output decreases with output power.
5. All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
6. A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	42.0" WXGA TFT LCD

BUYER	
MODEL	

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	LC420W02
SUFFIX	SLA1 (Lead Free)

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE / DATE
/	
/	
/	

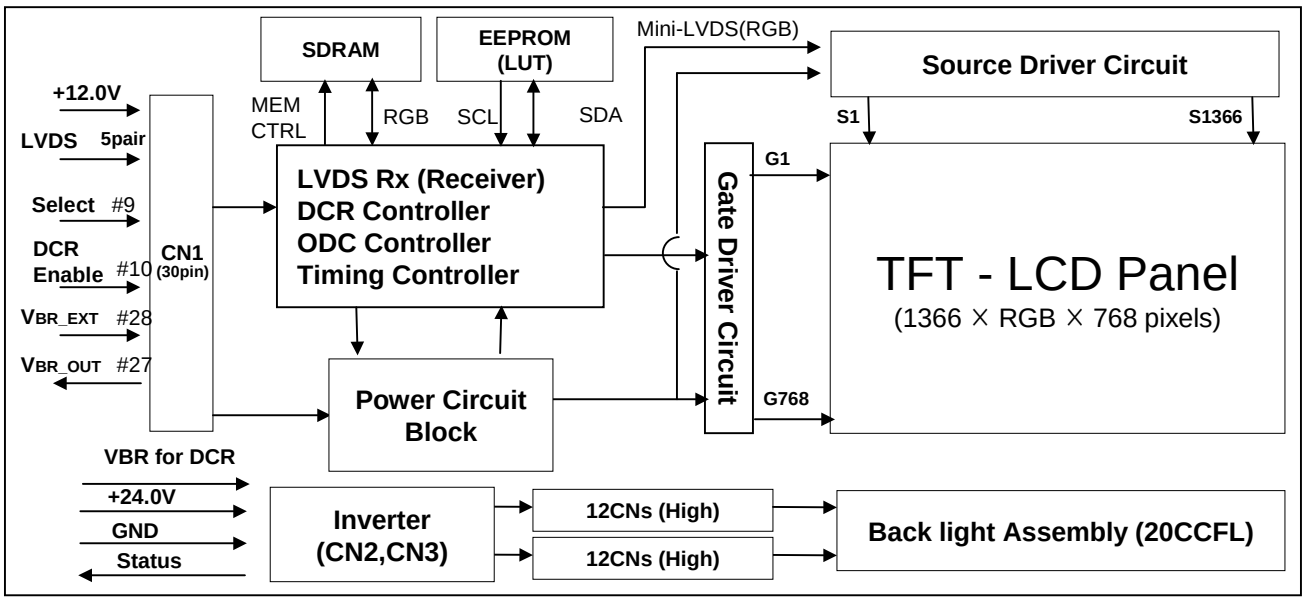
Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE / DATE
J.J Kim / S. Manager	01. 3. 03
REVIEWED BY	
K. S Choi / Manager	01-3-03
PREPARED BY	
S. W Kwag / Engineer	01-3-03

TV Products Development Dept.
LG. Philips LCD Co., Ltd

1. General Description

The LC420W02 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.0 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus presenting a palette of more than 16.7M(true) colors.
It has been designed to apply the 8-bit 1-port LVDS interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.308mm) diagonal
Outline Dimension	1006 mm(H) x 610 mm(V) x 56 mm(D) (Typ.)
Pixel Pitch	0.227mm x 0.681mm x RGB
Pixel Format	1366 horiz. by 768 vert. Pixels RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Luminance, White	500 cd/m^2 (Center 1-point) (Typ.)
Viewing Angle (CR>10)	Viewing Angle Free (R/L 178 (Typ.), U/D 178 (Typ))
Power Consumption	Total 167.7W (Typ.) (Logic=5.7W, Inverter=162W [I_{BL}=6.5mA])
Weight	14.5Kg (Typ.)
Display Operating Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer

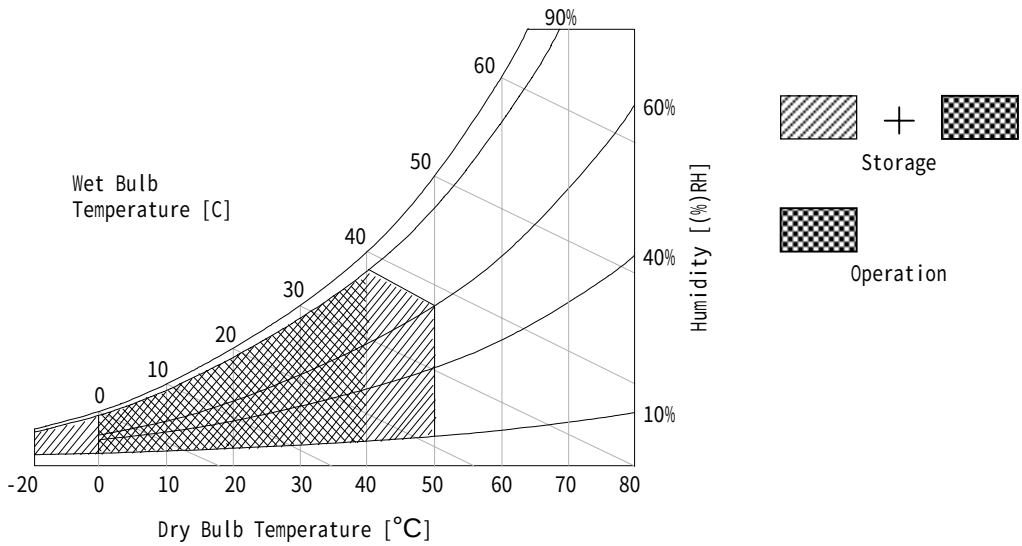
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Remark
			Min	Max		
Power Input Voltage	LCD circuit	V_{LCD}	-0.3	+14.0	V_{DC}	at 25 ± 2 °C
	Inverter	V_{BL}	21.6	+27.0	V_{DC}	
Inverter Control Voltage	ON/OFF	V_{OFF}/V_{ON}	-0.30	+5.25	V_{DC}	
	Brightness	V_{BR}	0.0	+5.0	V_{DC}	
Operating Temperature		T_{OP}	0	+40	°C	Note 1
Storage Temperature		T_{ST}	-20	+50	°C	
Operating Ambient Humidity		H_{OP}	10	90	%RH	
Storage Humidity		H_{ST}	10	90	%RH	

Note 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

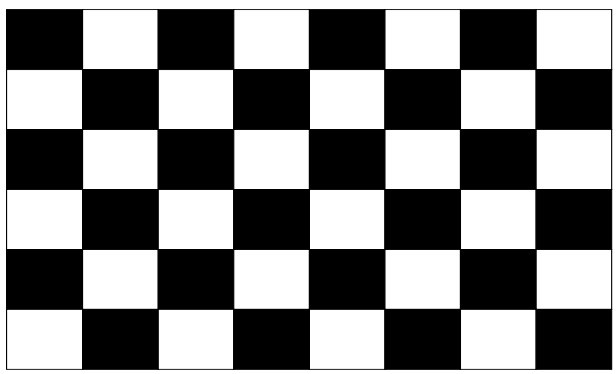
It requires two power inputs. One is employed to power for the LCD circuit. The other input power for the CCFL/Backlight is to power inverter.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Circuit :						
Power Input Voltage	V_{LCD}	11.4	12.0	12.6	V_{DC}	
Power Input Current	I_{LCD}	-	475	618	mA	1
		-	680	884	mA	2
Power Consumption	P_{LCD}		5.7	7.42	Watt	1
Rush current	I_{RUSH}	-	-	3.0	A	3

Note : 1. The specified current and power consumption are under the V_{LCD}=12.0V, 25 ± 2°C, f_V=60Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power input is 1ms (min.).

White : 255Gray
Black : 0Gray



Mosaic Pattern(8 x 6)

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter			Symbol	Values			Unit	Notes
				Min	Typ	Max		
Inverter :								
Power Supply Input Voltage			V_{BL}	22.8	24.0	25.2	Vdc	1
Power Supply Input Voltage Ripple				-0.2		0.2	Vp-p	
Power Supply Input Current			I_{BL}	-	6.75	7.2	A	
Power Consumption			P_{BL}	-	162	172.8	W	
Input Voltage for Control System Signals	Brightness Adjust		V_{BR}	0.0	-	3.3	Vdc	2
	On/Off	On	V on	4.0	-	5.0	Vdc	
		Off	V off	-0.3	0.0	0.5	Vdc	
Lamp :								
Life Time				50,000			Hrs	3

Notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 120 minutes at 25±2°C
   The specified current and power consumption are under the typical supply Input voltage 24V and Vbr 3.3V, it is total power consumption.
   The ripple voltage of the power supply input voltage is under 0.2 Vp-p.
   LPL recommend Input Voltage is 24.0V ± 5%.
2. Brightness Control.
   This V_{BR} Voltage control brightness.

V_{BR} Voltage	Function
3.3V	Maximum Brightness (100%)
0V	Minimum Brightness.(25%)

3. The life is determined as the time at which luminance of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2°C.
   Specified value is when lamp is aligned horizontally.

3-2. Interface Connections

This LCD module employs two kinds of interface connection, a 30-pin connector is used for the module electronics and two 12-pin connectors are used for the integral backlight system.

3-2-1. LCD Module

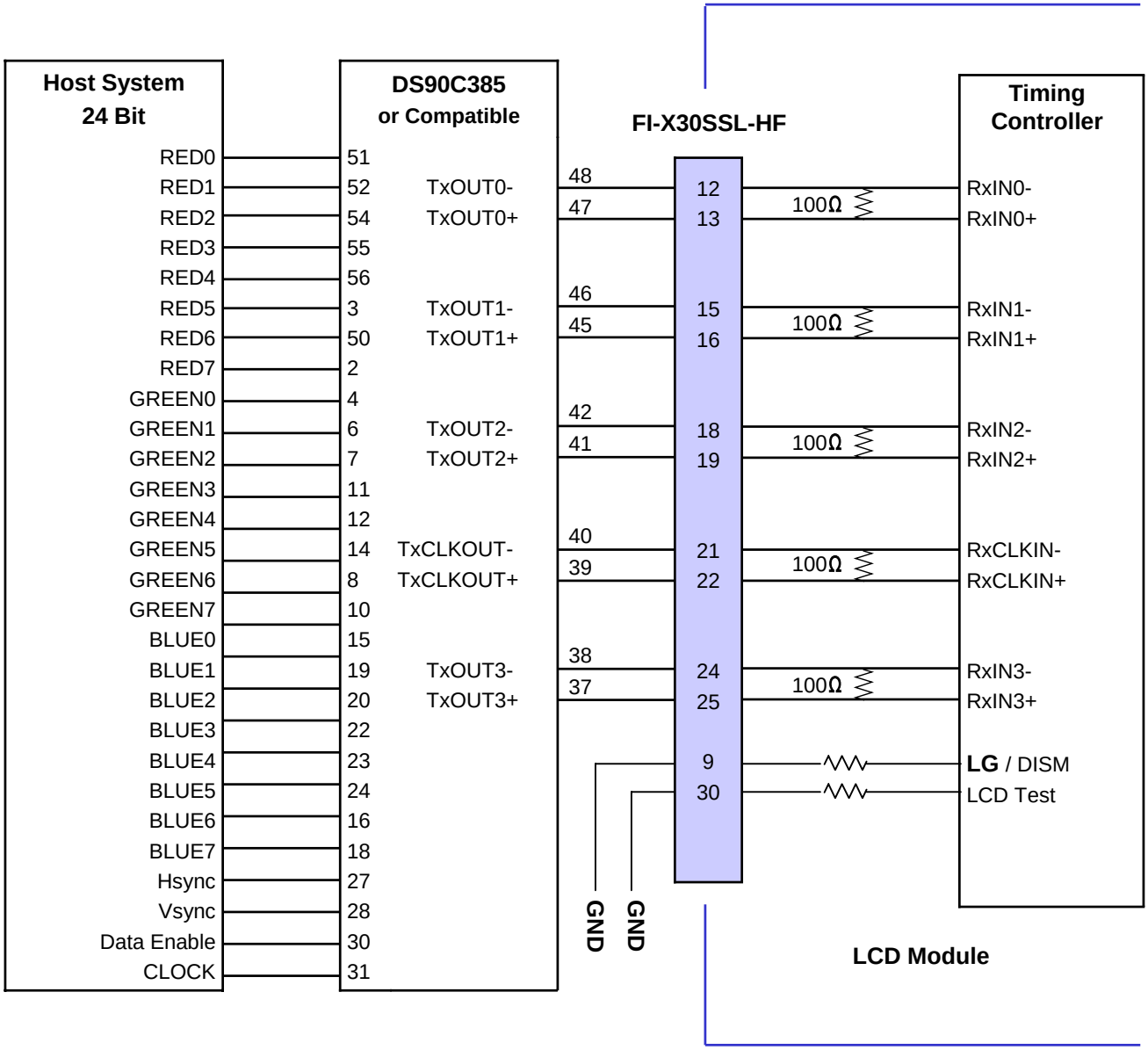
- LCD Connector(CN1) : FI-X30SSL-HF (Manufactured by JAE) or Equivalent
- Mating Connector : FI-30C2L (Manufactured by JAE) or Equivalent

Table 4. MODULE CONNECTOR(CN1) PIN CONFIGURATION

Pin No.	Symbol	Description	Note
1	VLCD	Power Supply +12.0V	
2	VLCD	Power Supply +12.0V	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	Select	Select LVDS Data format	1
10	DCR Enable	Dynamic CR Enable ('L ' = Disable , 'H' = Enable)	2
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	VBR_OUT	VBR output form LCD module	
28	VBR_EXT	External VBR input from System to LCD module	
29	GND	Ground	
30	GND	Ground	3

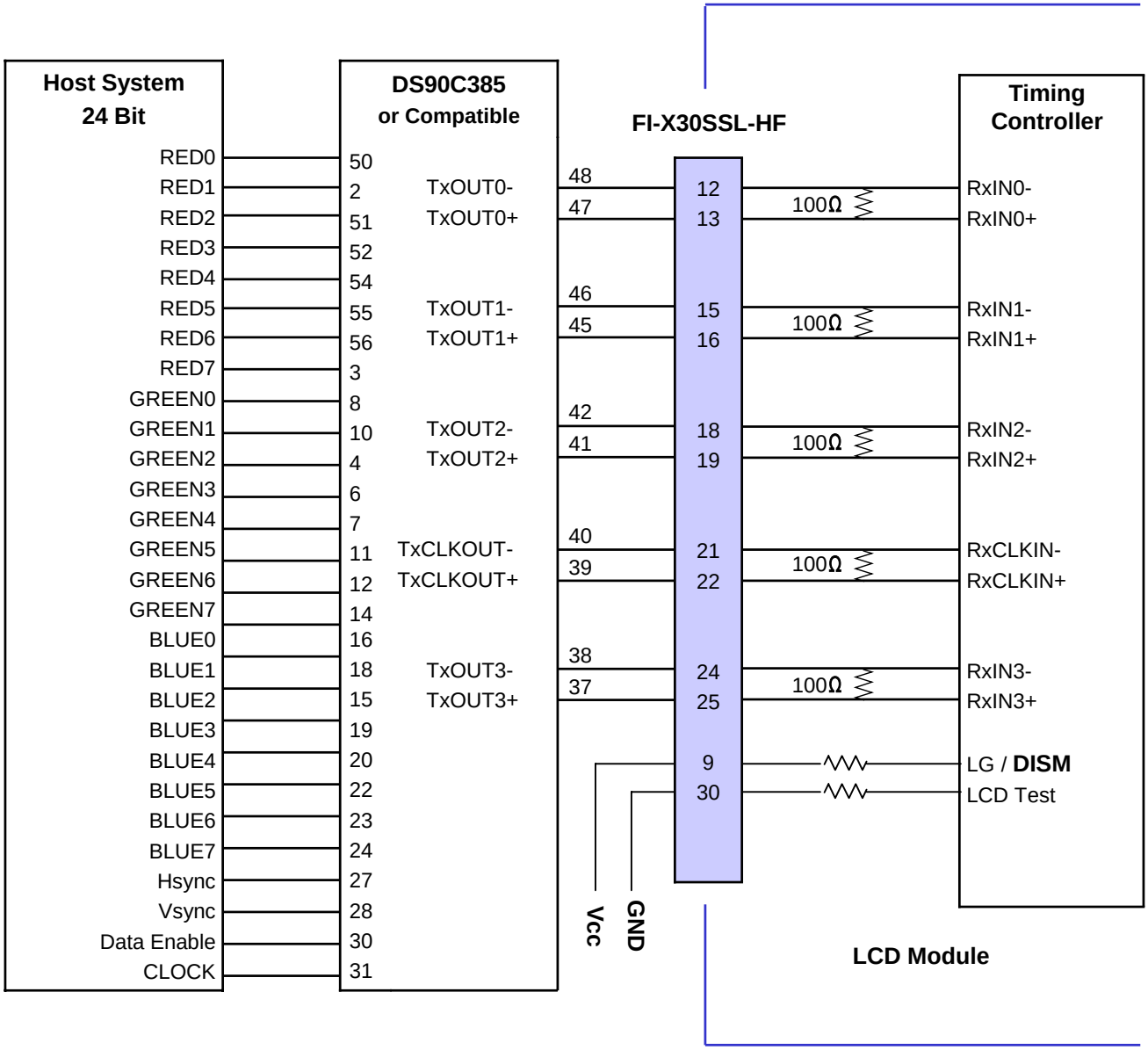
Note: 1. The pin no 9 is an option pin for DISM or LG format. (LG Format = "GND" / DISM Format ="VCC")
Please refer to page 9 and 10 for further details
2. The pin no 10 is an option pin for DCR Function (Enable = "VCC" / Disable ="GND")
3. The pin no 30 is LCD Test option.
LCM operates "AGP" (Auto Generation Pattern) or "NSB" (No Signal Black) is case that LVDS signals are out of frequency or abnormal condition in spite of 12 volt power supply.
LPL recommends "NSB". (AGP : "VCC" or "OPEN" / NSB : "GND")
4. All GND (ground) pins should be connected together, which should be also connected to the LCD module's metal frame.
5. All V_{LCD} (power input) pins should be connected together.
6. Input Levels of LVDS signals are based on the IEA 664 Standard.

Table 5. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER (Pin9="L")



Note: 1. The LCD Module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible**)**
3. '7' means MSB and '0' means LSB at R,G,B pixel data.

Table 6. REQUIRED SIGNAL ASSIGNMENT FOR LVDS TRANSMITTER (Pin9="H")



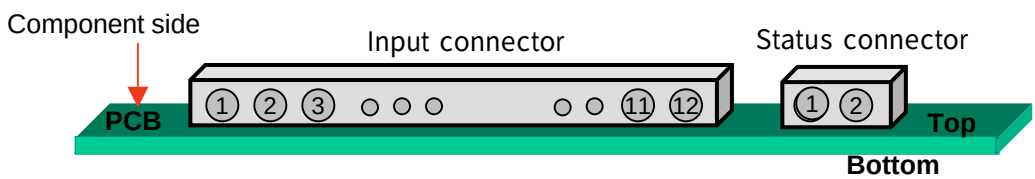
Note: 1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (DS90C385 or Compatible**)**
3. '7' means MSB and '0' means LSB at R,G,B pixel data.

3-2-2. Backlight Inverter

- Inverter Connector : S12B-PH-SM3(manufactured by JST) or Equivalent
- Mating Connector : PHR-12 or Equivalent
  Status Connector
-Inverter Connector : 20022WR-02A00(manufactured by Yeon Ho co., Korea)
-Mating Connector : 20022HR-02S00(manufactured by Yeon Ho co., Korea)

Table 7. INVERTER CONNECTOR PIN CONFIGULATION

Pin No	Symbol	Description	Master	Slave	Note
1	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
2	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
3	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
4	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
5	V_{BL}	Power Supply +24.0V	V_{BL}	V_{BL}	
6	GND	POWER GND	GND	GND	
7	GND	POWER GND	GND	GND	
8	GND	POWER GND	GND	GND	1
9	GND	POWER GND	GND	GND	
10	GND	POWER GND	GND	GND	
11	V_{BR}	0V ~ 3.3V	V_{BR}	Don't care	2
12	On/Off	0V ~ 5.0V	On/Off	Don't care	3
Option Pin(Lamp Open Status Detection)					
1	GND	POWER GND	GND		
2	Status	Upper 3.0V(Normal), Under 0.7V(Abnormal)	Status		



S12B-PH-SM3-TB
(JST : Japan Solderless Terminal Co.,Ltd.)

Note : 1. GND should be connected to the LCD module's metal frame.

2. Minimum Brightness : V_{BR} = 0.0V
   Maximum Brightness : V_{BR} = 3.3V

3. V_{ON} : 4.0 ~ 5.0V
   V_{OFF} : -0.3 ~ 0.5V

3-3. Signal Timing Specifications

Table 8 and Table9 show the signal timing required at the input of the LVDS transmitter. All of the interface signal timing should be satisfied with the following specification for normal operation.

Table 8. TIMING TABLE for NTSC

ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK Period		t_{CLK}	13.1	13.8	14.5	nsec	
DCLK Frequency		f_{CLK}	68.3	72.4	75.1	MHz	
Vertical	Frequency	f_V	57	60	63	Hz	
	Valid	t_{VV}	-	768	-	Line	
	Blank	$t_{VT} - t_{VV}$	8	22	295	Line	
	Total	t_{VT}	776	790	1063	Line	
Horizontal	Frequency	f_H	45	47.4	50	KHz	
	Valid	t_{HV}	-	1366	-	t_{CLK}	
	Blank	$t_{HT} - t_{HV}$	90	162	410	t_{CLK}	
	Total	t_{HT}	1456	1528	1776	t_{CLK}	

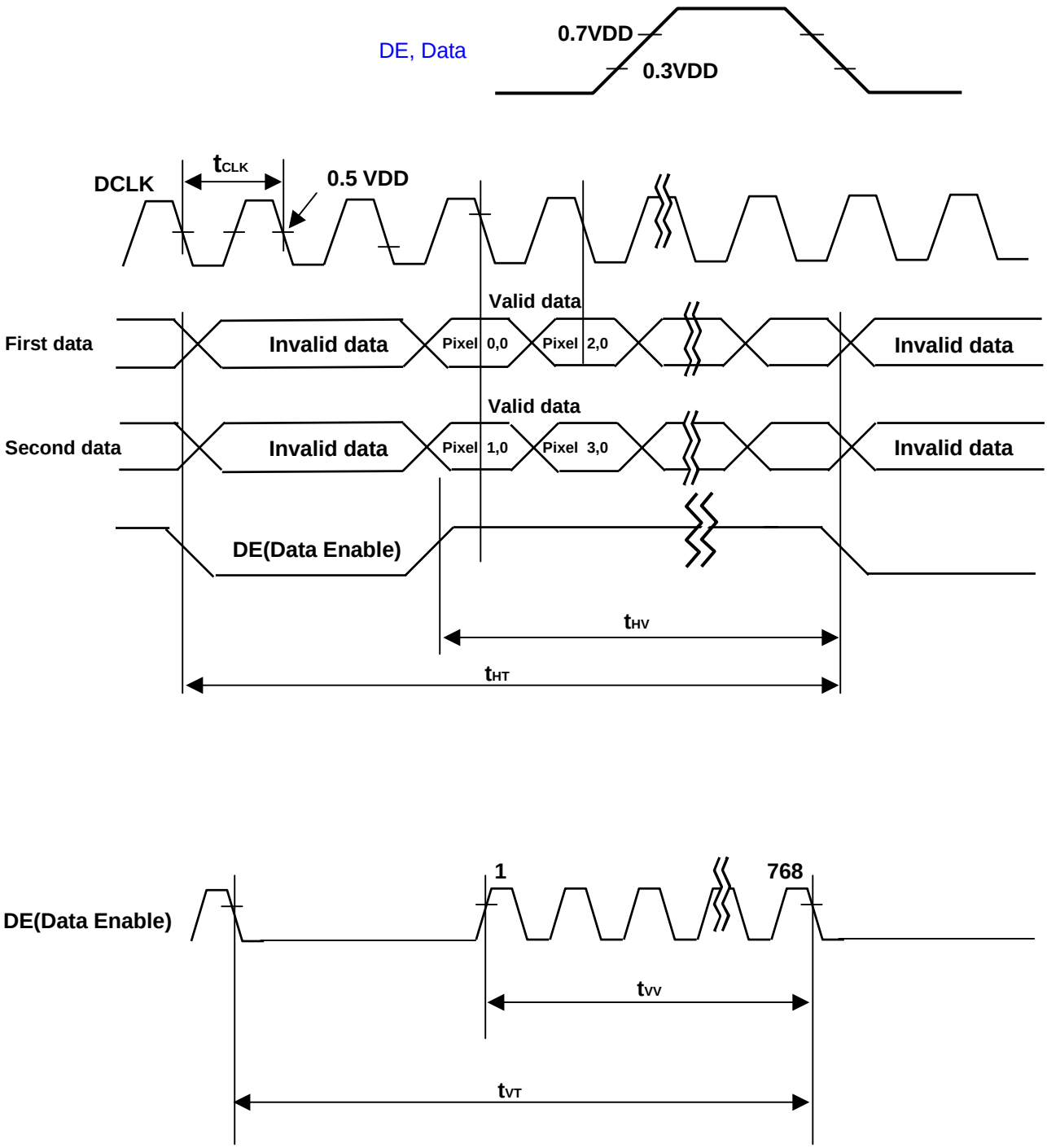
Table 9. TIMING TABLE for PAL

ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK Period		t_{CLK}	13.0	13.8	14.6	nsec	
DCLK Frequency		f_{CLK}	68.1	72.6	76.3	MHz	
Vertical	Frequency	f_V	47	50	53	Hz	
	Valid	t_{VV}	-	768	-	Line	
	Blank	$t_{VT} - t_{VV}$	8	182	295	Line	
	Total	t_{VT}	776	950	1063	Line	
Horizontal	Frequency	f_H	44.65	47.5	50.35	KHz	
	Valid	t_{HV}	-	1366	-	t_{CLK}	
	Blank	$t_{HT} - t_{HV}$	90	162	410	t_{CLK}	
	Total	t_{HT}	1456	1528	1776	t_{CLK}	

Note :

1. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate.
2. Above Timing Tables are only valid for DE Mode.

3-4. Signal Timing Waveforms



3-5. Color Data Reference

The brightness of each primary color(red,green,blue) is based on the 8-bit gray scale data input for the color. The higher binary input, the brighter the color. Table 10 provides a reference for color versus data input.

Table 10. COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...	...								...								...							
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	...	...								...								...							
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLUE (000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...	...								...								...							
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3-6. Power Sequence

3-6-1. LCD Driving circuit

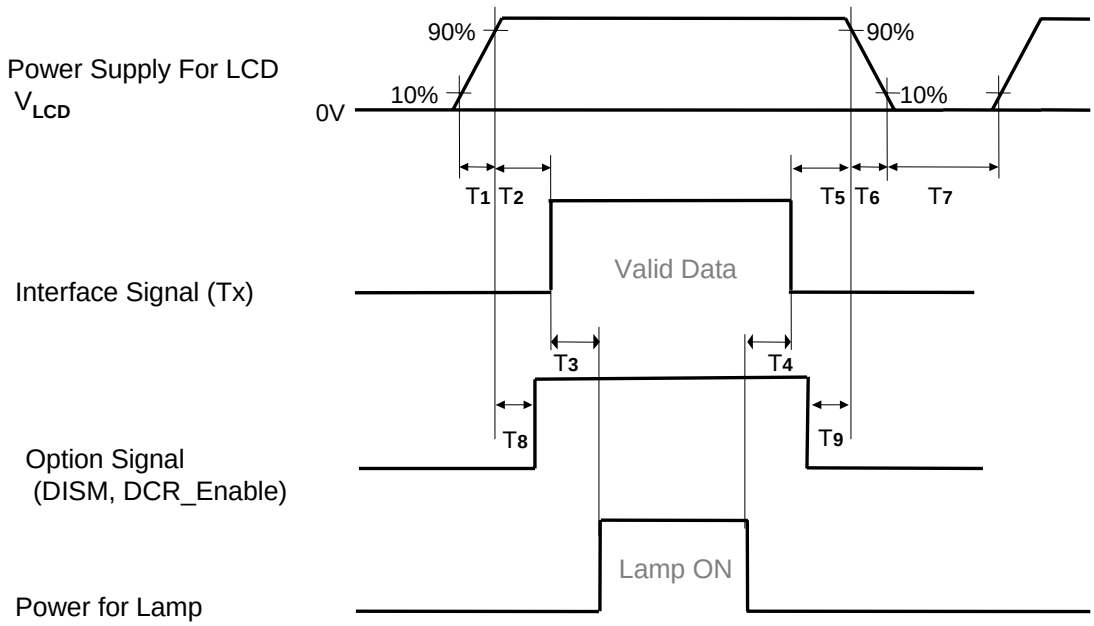
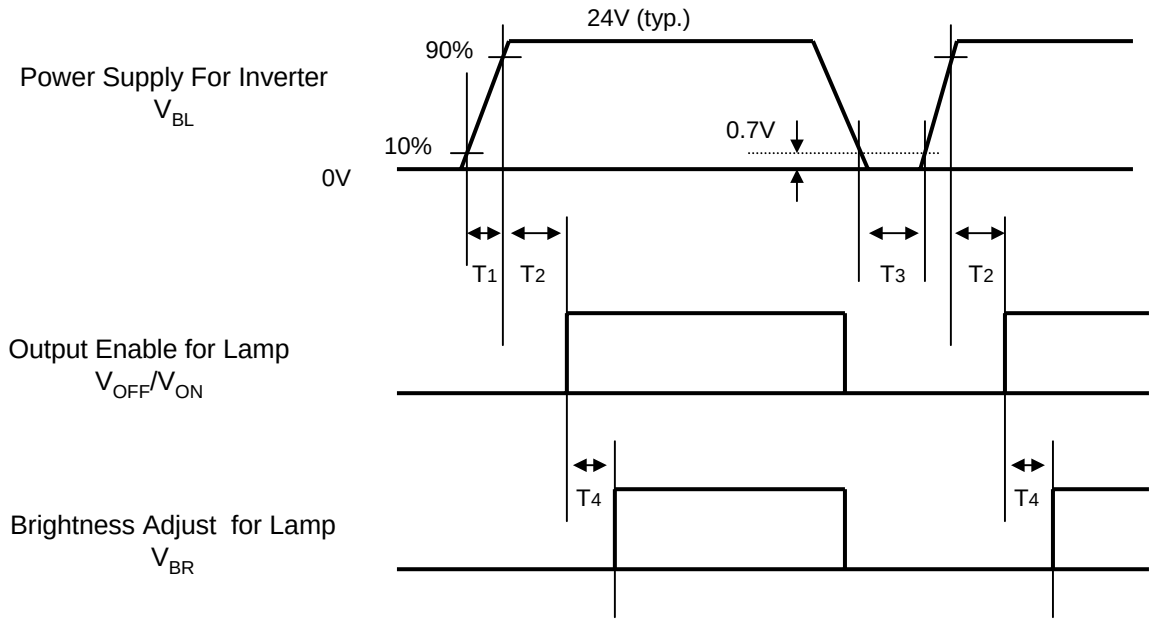


Table 11. POWER SEQUENCE

Parameter	Value			Unit
	Min	Typ	Max	
T1	1.0	-	20	ms
T2	5.0	-	50	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0.5	-	50	ms
T6	-	-	300	ms
T7	1.0	-	-	s
T8	0 < T8 < T2			ms
T9	0 < T9 < T5			ms

Note : 1. Please avoid floating state of interface signal at invalid period.
2. When the interface signal is invalid, be sure to pull down the power supply V_{LCD} to 0V.
3. The case when the T2/T5 exceed maximum specification, it operates protection pattern(Black pattern) till valid signal inputted. There is no reliability problem.
4. The T3/T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.

3-6-2. ON/OFF for Inverter



3-6-3. Deep condition for Inverter

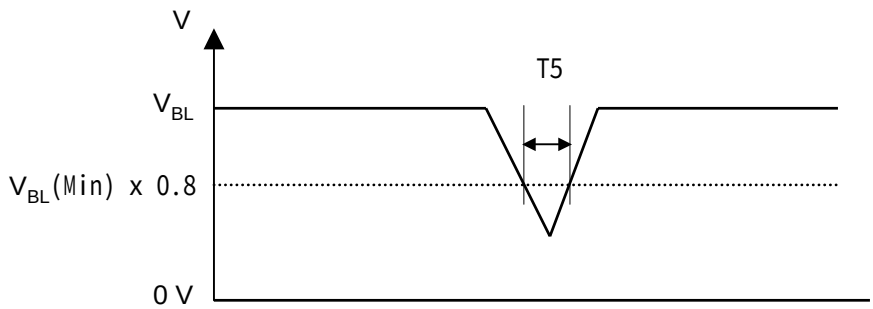


Table 12. POWER SEQUENCE FOR INVERTER

Parameter	Value			Unit	Remark
	Min	Typ	Max		
T1	20	-	-	ms	inverters connected condition
T2	500	-	-	ms	
T3	200	-	-	ms	
T4	0	-	-	ms	
T5	-	-	10	ms	V_{BL}(Min) x 0.8

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
It is presented additional information concerning the measurement equipment and method in FIG. 1.

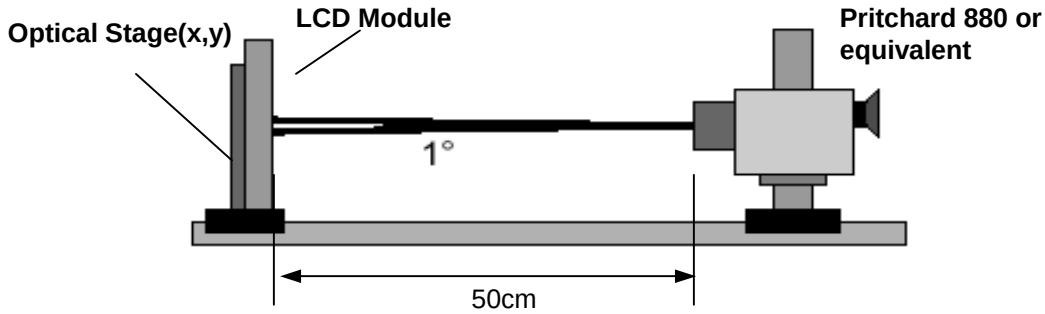


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 13. OPTICAL CHARACTERISTICS Ta= 25±2°C, V_{LCD}=12.0V, fv=60Hz, Dclk=72.4MHz, V_{BR}=3.3V

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	600	800			1
		CR with DCR	1200	1600			
Surface Luminance, white		L_{WH}	400	500		cd/m^2	2
Luminance Variation		δ_{WHITE} 5P			1.3		3
Response Time (Gray to Gray)	Rise Time	Tr_R	-	8	12		
	Decay Time	Tr_D		10	14		
	G to G		-	8	12	ms	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.630	Typ +0.03		
		Ry		0.343			
	GREEN	Gx		0.275			
		Gy		0.607			
	BLUE	Bx		0.147			
		By		0.068			
	WHITE	Wx		0.281			
		Wy		0.293			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	85	89	-	degree	5
	x axis, left (ϕ=180°)	θl	85	89	-		
	y axis, up (ϕ=90°)	θu	85	89	-		
	y axis, down (ϕ=270°)	θd	85	89	-		
Gray Scale		Without DCR					6
		With DCR					

Note :

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 2.

3. The variation in surface luminance , δ WHITE is defined as :

$$\delta \text{ WHITE(5P)} = \text{Maximum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}) / \text{Minimum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5})$$

Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 2.

4. Response time is the time required for the display to transition from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information see the FIG. 3. (N<M)

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.

6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 14.

Table 14. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)	Luminance [%] (Typ) with DCR
L0	0.11	0.06
L15	0.19	0.16
L31	1.08	0.63
L47	2.07	1.68
L63	4.51	3.54
L79	7.75	6.41
L95	12.05	10.82
L111	17.06	16.74
L127	22.36	22.00
L143	28.21	27.44
L159	35.56	34.62
L175	43.96	42.94
L191	53.00	51.94
L207	63.37	62.25
L223	74.66	73.66
L239	88.17	87.05
L255	100	100

Measuring point for surface luminance & measuring point for luminance variation

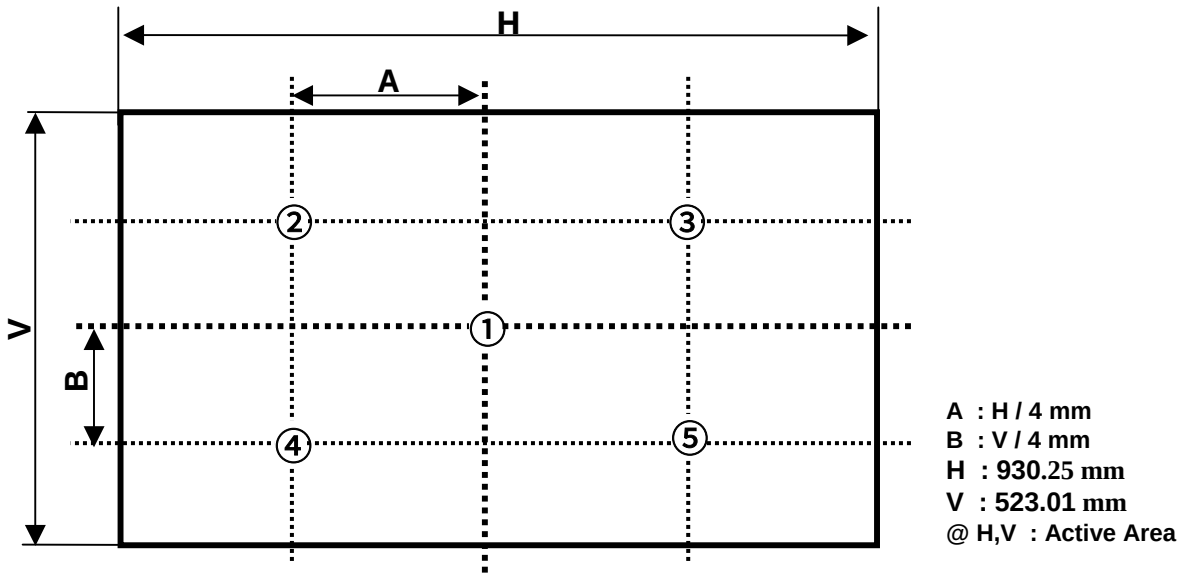


FIG.2 Measure Point for Luminance

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

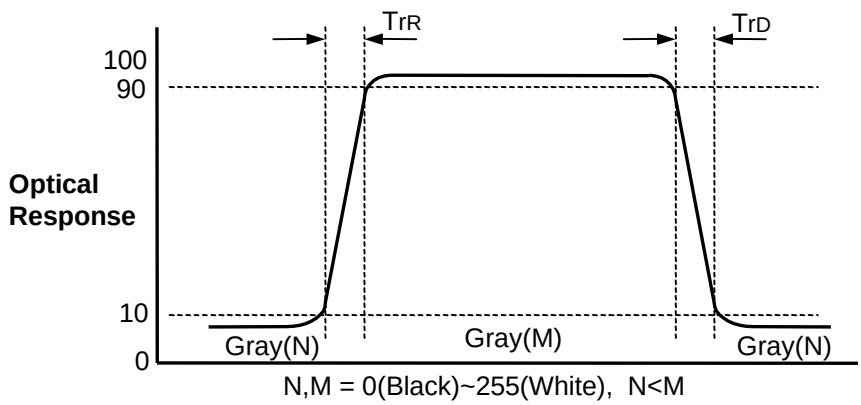


FIG.3 Response Time

Dimension of viewing angle range

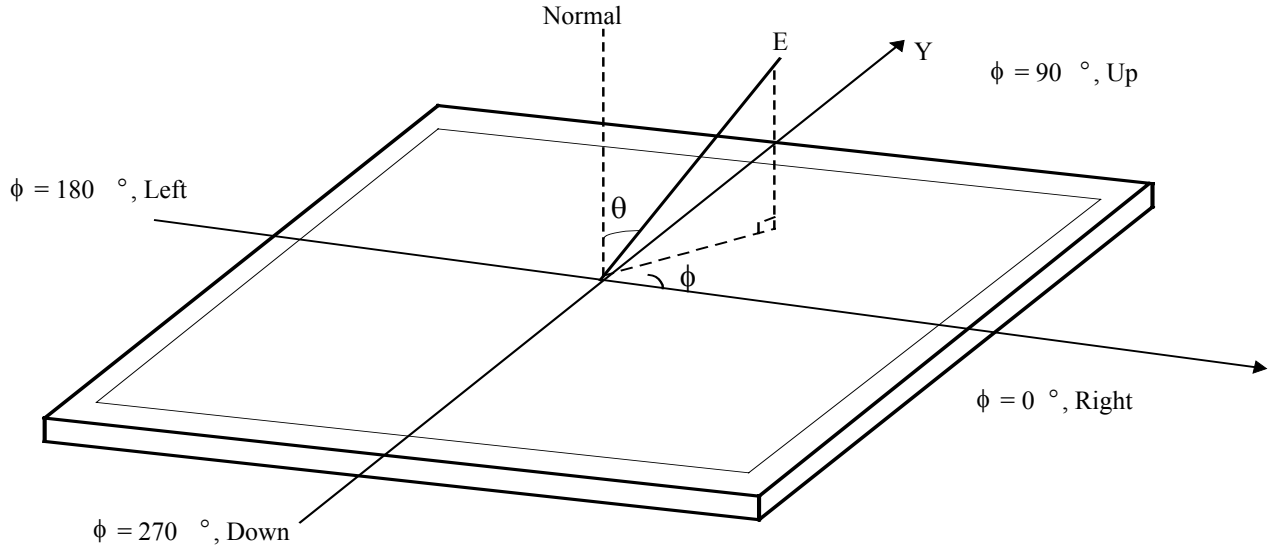


FIG.4 Viewing Angle

5. Mechanical Characteristics

The contents provide general mechanical characteristics. In addition the figures in the next page are detailed mechanical drawing of the LCD module.

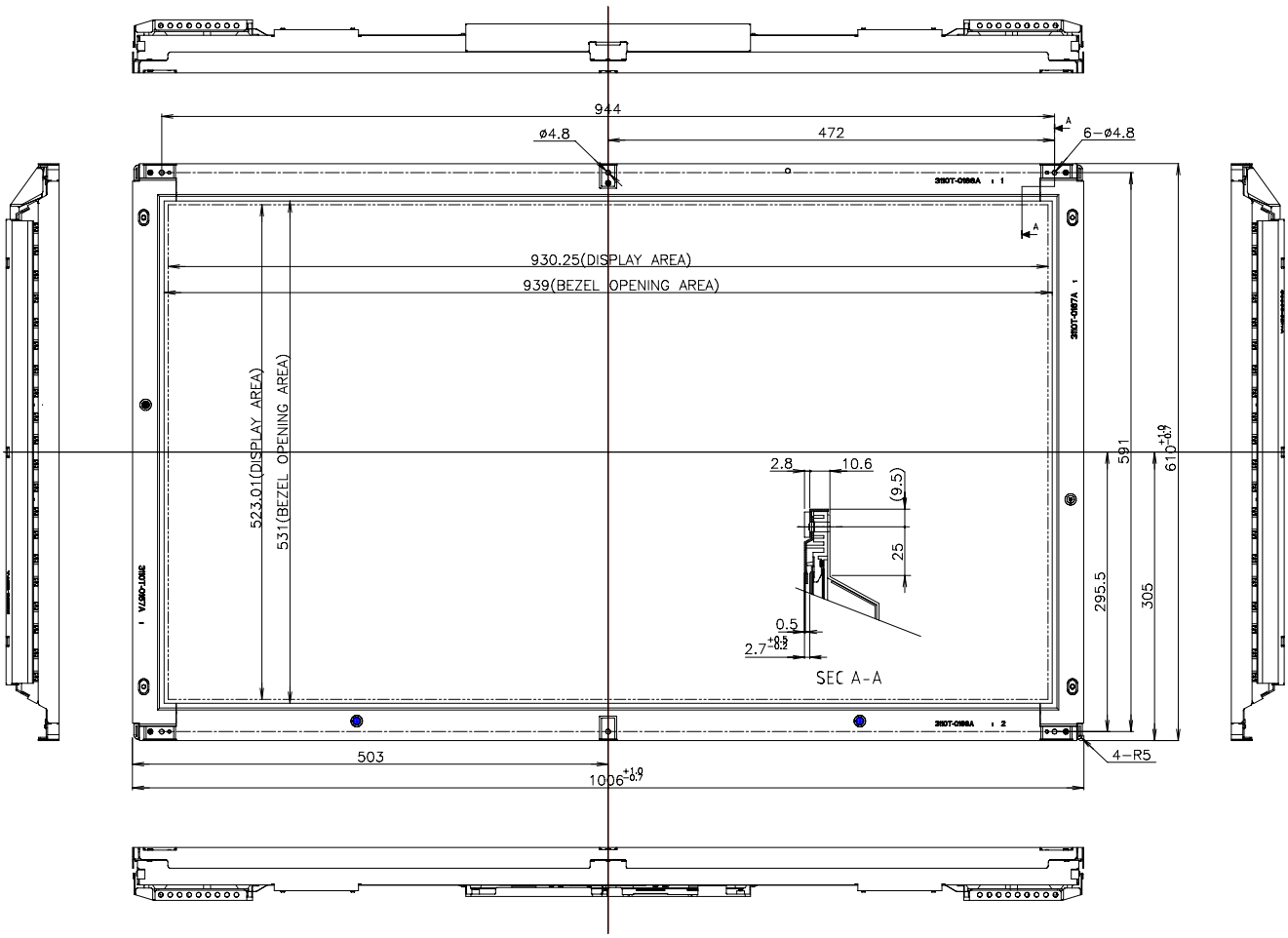
Table 15. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	1006.0 mm
	Vertical	610.0 mm
	Depth	56.0 mm
Bezel Area	Horizontal	939.0 mm
	Vertical	531.0 mm
Active Display Area	Horizontal	930.25 mm
	Vertical	523.01 mm
Weight	14.5Kg (Typ.) , 15.5Kg (Max.)	
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer	

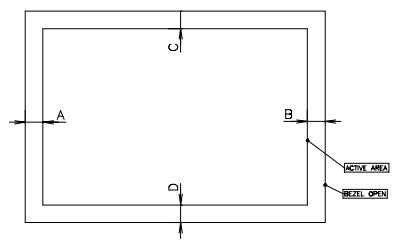
Note : Please refer to page22 and 23 for mechanic drawings in terms of tolerance.

Product Specification

<FRONT VIEW>

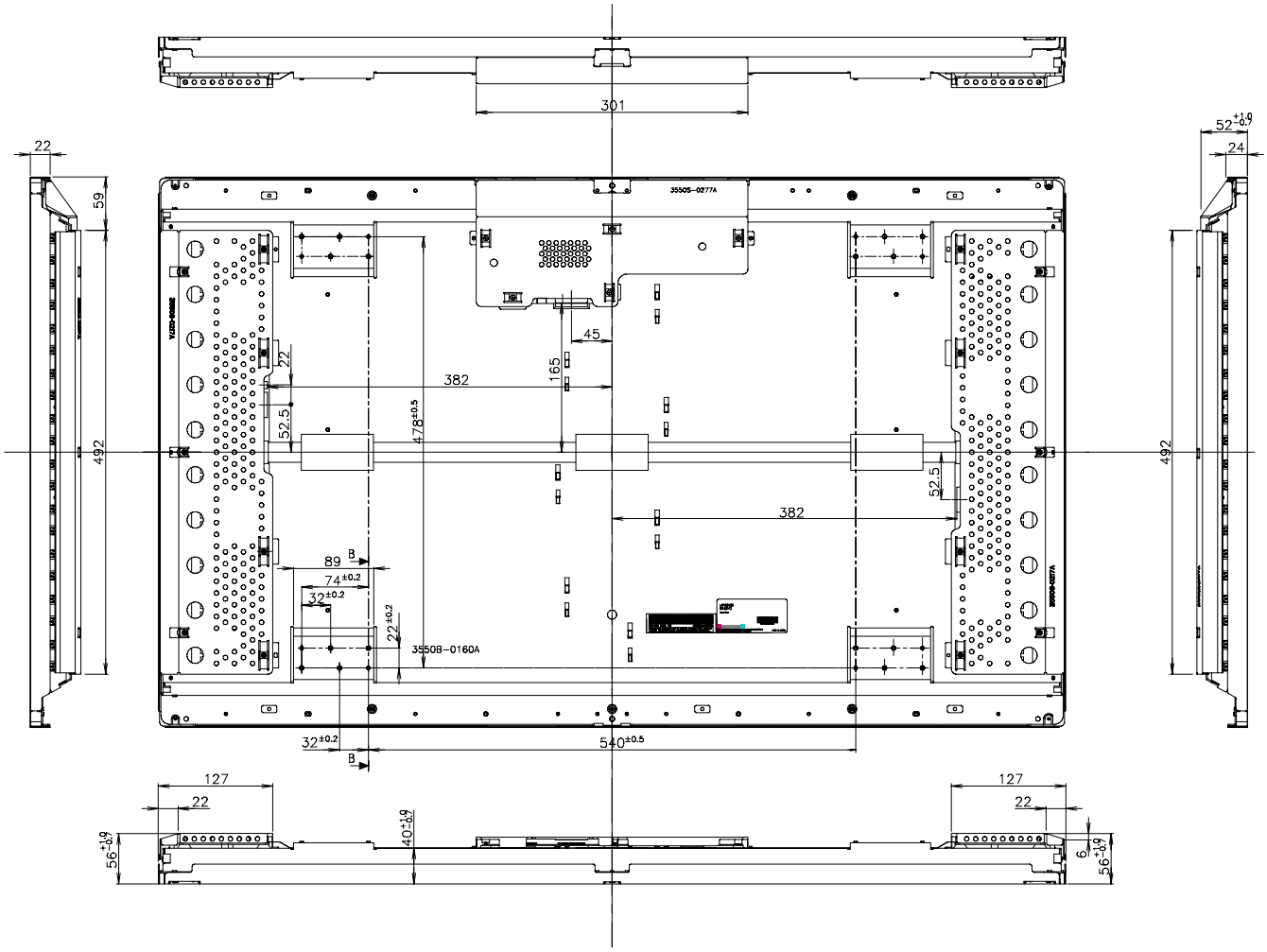


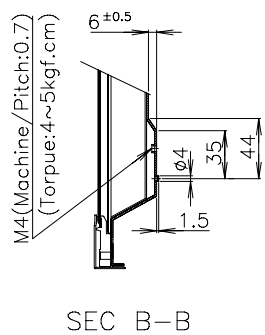
NOTE
1. UNSPECIFIED TOLERANCE IS ±1.0 mm
2. GAP BETWEEN TOP CASE AND GLASS IS $0.7^{+0.5}_{-0.2}$
3. TILT AND A PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA ARE AS FOLLOW.
   1) X-DIRECTION : | A-B | ≤ 1.5mm
   1) Y-DIRECTION : | C-D | ≤ 1.5mm



Product Specification

<REAR VIEW>





SEC B-B

6. Reliability

Table 16. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 50°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 40°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z, 30 min One time each direction
6	Shock test (operating)	Shock level : 50Grms Waveform : half sine wave, 11ms Direction : ±X, ±Y, ±Z One time each direction
7	Humidity condition Operation	Ta= 40 °C ,90%RH
8	Altitude operating storage / shipment	0 - 14,000 feet(4267.2m) 0 - 40,000 feet(12192m)

7. International standards

7-1. Safety

a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,
Standard for Safety of Information Technology Equipment.
b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,
Standard for Safety of Information Technology Equipment.
c) EN 60950-1: 2001, First Edition.
European Committee for Electrotechnical Standardization(CENELEC)
European Standard for Safety of Information Technology Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998
(Including A1: 2000)

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 10 pcs

b) Box Size :1140 mm X 1000 mm X 810 mm.

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it causes metallic foreign material and deal LCM a fatal blow)
(9) Please do not set LCD module on its edge.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

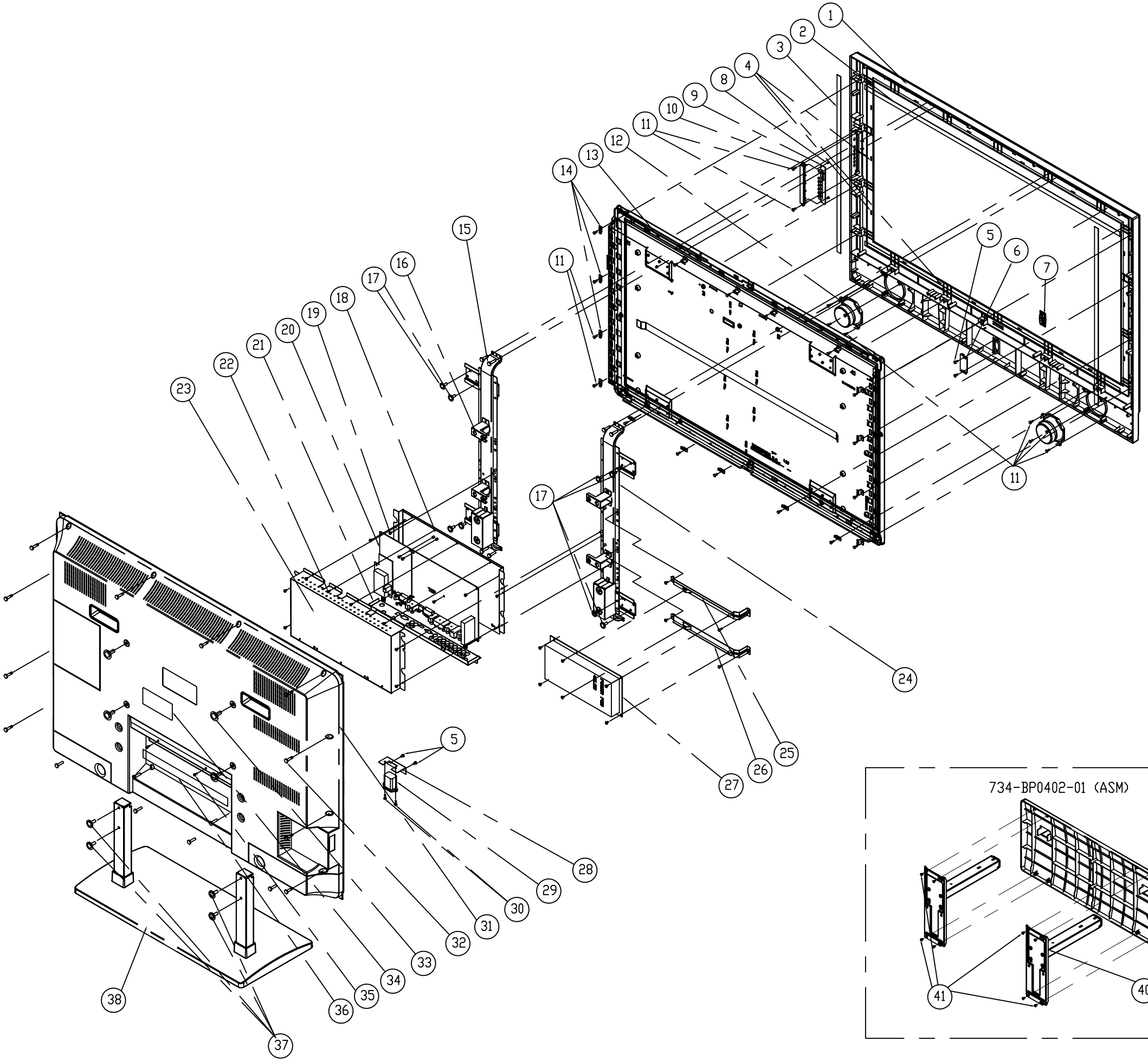
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

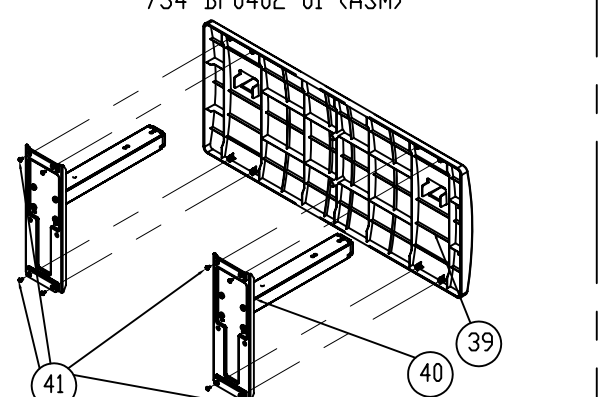
(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY

DWG. REV.	ZONE	DESCRIPTION	DATE	REVISOR



734-BP0402-01 (ASM)



ITEM	PART NO.	DESCRIPTION	QTY	REMARK
45				
44				
43				
42				
41	612-300108-00	S-TAP.SCREW WHR 3X8	8	
40	712-BP0402-01	STAND SUPPORT ASSY BP04 W=EMBO BLACK	2	ASM
39	231-BP0401-01AR	STAND COVER BP04 SILVER R	1	
38	734-BP0402-01	PLASTIC STAND SILVER FOR LCT4260 CB=4680H W/O PACKING	1	ASM
37	60D-508015-00	MACH SCREW W/SPRING WASHER M5X40(BOSH) BLACK ZN PLATE	4	
36	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" D-MTB08E USA P	1	
35	602-305008-00	MACH SCREW PAN-WASHER M3X8 BZN+Ni	4	
34	560-L42AD01-01AP	MODEL LABEL ILO LCT4260HS D-MTB08E AUS USA P	1	
33	602-601010-00	MACH SCREW PAN WASHER M5.6X10P3BN BLACK Zn PLATED	4	
32	614-400412-00	S-TAP.SCREW BID 4X12	26	
31	202-L42AD01-01AA	CABINET BACK BLACK LCT426D W/O POWER SWITCH AND DVD A	1	
30	601-305008-00	MACH.SCREW CTS 3X8 BZN +H	2	
29	E3421-925118	WIRE ASSY SPED/PRES L250H 5V 32V 250MA, POWER MT8202	1	
28	426-L37AD02-01S	AC JACK BRACKET	1	
27	E7801-P02004	POWER SWITCH	1	
26	G429-L42AE02-01SA	PCB ASSY PSU BOARD NEGMEET MULTIPWL FOR 42"LCD	1	
25	G429-L42AE01-01SA	ROHS POWER BKT TOP	1	
24	713-L42AE02-01	MAIN BKT ASSY LEFT L42AE	1	ASM
23	483-L32AB32-01S	SHIELDING COVER	1	
22	602-305004-10	MACH. SCREW PAN-WASHER M3X14 NSP +H	8	
21	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1	
20	E3761-058010-6	PCB VO 250X175 MAIN MT8202 4LA YER	1	
19	602-305006-10	MACH.SCREW WHR 3X6	24	
18	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1	
17	60D-407008-10	MACH.SCREW W/SPRING WASHER M4X8.7P3BSN ZNP	8	
16	713-L42AE01-01	MAIN BKT ASSY RGHT L42AE	1	ASM
15	614-400412-00	S-TAP.SCREW BID 4X12	26	
14	G429-L32AE01-01SA	ROHS Z BKT EB H=9.0MM	14	
13	E6203-42PD02	DISPLAY LCD 42" LPL WXGA TFT LC420WX2-SLA6	1	
12	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2	
11	614-300110-10	S-TAP.SCREW BID 3X10	26	
10	277-137AE01-02AS	FUNCTION KNOB SILVER S	1	
9	E3701-065010	PCB VO KEY SINGLE0280X2760 0 IN X=4X3=12MM FOR LCT426E	1	
8	610-260208-10	S-TAP.SCREW RND 2.6X8	2	
7	459-L32AD01-01	REMOTE LENS ASS'Y FOR ILO	1	
6	E3701-051060	PCB VO REMOTE 34X20 FOR 32ILO TV+DVD TV FUNCTION	1	
5	614-300107-00	SELF TAPPING SCREW BINDING HEAD 3.0X7.8	4	
4	379-421D02-01	RUBBER 3M6 FOR 42ID SPEAKER 4.2X80X50X6.6X80 W/ADHESIVE	17	
3	521-550155-01	FELT PAPER 550X15X0.5MM W/ADHESIVE	2	
2	521-95015-01	FELT PAPER 950X15X0.5MM W/ADHESIVE	2	
1	200-L42AD1201-01AA	FRONT CABINET ILO SILVER/BLACK	1	

DRAWN.						
CHECKED						
APPRD.						
3rd ANGLE PROJECTION						

TOLERENCE UNLESS OTHERWISE SPECIFIED
0 MM~8 MM ± 0.1
8 MM~25MM ± 0.15
25MM~80MM ± 0.2
80MM~250MM ± 0.3
250MM~ABOVE ± 0.6
ANGULAR: ± 1°

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE LCT422DAIA1PS-A01

MODEL NO. LCT422D

A2 | PART NO. EXP-L42DD01-01 | DWG. NO. L422DEXP1

SCALE NIL | QTY. | SHEET 1 OF 1

Spare part list for LCT42HA36

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
	LCT422DAIA1PS-A01	ILO LCT422D (LCT42HA36) S-MT8202 LPL(LC420W02-SLA1 V1.0) AC120V/60HZ USA SILVER/BLACK			
1>	510-L42AE01-05AK	CARTON BOX ILO LCT42HA36 S-MT8202 LPL USA K	1.000000	Piece	K
2>	518-421D01-01K	BOTTOM BOX 421D K	1.000000	Piece	K
3>	580-L422D1A-02AP	IB E FOR ILO LCT42HA36 TV+DTV W/O PIP LPL S-MTK8202 USA	1.000000	Piece	K
4>	E3407-081001	CORD FFC P0.5 50P L=110 B-0.5-50X110-4(8)X4(8)-0.3X0.035	1.000000	Piece	K
5>	E7501-056104	REMOTE CONTROL K001 "ILO" 44KEYS MT8202 LCD TV USA BLACK	1.000000	SET	K
6>	E7801-P02004	PCB ASSY PSU BOARD MEGMEET MLT198L FOR 42"LCD AC110-240V OUTPUT 5V/12V/24V/5VSB 300W	1.000000	SET	K
7>	771EL37AD03-04	PCB ASS'Y MAIN S-MT8202 FOR LCT37" LPL	1.000000	SET	K
8>	771S42D102-02	ATSC TUNER PCB ASS'Y (MT5111CE) W/O MAX3232	1.000000	SET	K
9>	200-L42AD02-01AA	FRONT CABINET ILO SILVER/ BLACK LCT42HA36 LPL A	1.000000	Piece	S
10>	202-L42AD01-01AA	CABINTE BACK BLACK LCT42AD W/ O POWER SWITCH AND DVD A	1.000000	Piece	S
11>	231-BP0401-01AR	STAND COVER BP04 SILVER R	1.000000	Piece	S
12>	310-041204-01V	POLYBAG 4"X12"X0.04 AV	1.000000	Piece	S
13>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1.000000	Piece	S
14>	310-504505-01T	POLYBAG 50"X45"X0.5MM W/MU/TI LANGUAGE WARING &RECYCLE &HOLE	1.000000	Piece	S
15>	370-42D102-01	PAD CORD SPONG FOR SPK	1.000000	Piece	S
16>	379-L42AD01-01	RUBBER BAR 1.8X3.0X15MM WITH ADHESIVE	1.000000	Piece	S
17>	426-L37AD02-01S	AC JACK BRACKET	1.000000	Piece	S
18>	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1.000000	Piece	S

19>	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1.000000	Piece	S
20>	483-L32AB32-01S	SHIELDING COVER	1.000000	Piece	S
21>	486-L32AD01-01	NAME PLATE ILO SILVER/BLACK	1.000000	Piece	S
22>	553-002007-25A	SHIELD GASKET 20X7X2.5MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
23>	560-L42AD01-01AP	MODEL LABEL ILO LCT42HA36 S-MT8202 AUO USA P	1.000000	Piece	S
24>	563-119-	SERIAL NO. LABEL	1.000000	Piece	S
25>	568-P46T02-02	WARNING LB ENG 42SF NIL	1.000000	Piece	S
26>	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" S-MT8202 USA P	1.000000	Piece	S
27>	579-42D102-09	SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
28>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
29>	579-L27AD09-01	CAUTION LABEL ENG AKAI	1.000000	Piece	S
30>	579-L32AD09-02AP	FCC STATEMENT LABEL 77X20MM	1.000000	Piece	S
31>	579-L42AD01-01AP	BAR CODE LABEL ILO LCT42HA36 USA P	2.000000	Piece	S
32>	590-L42AD01-01AP	WARRANTY CARD ILO ENG LCT42HA36 USA P	1.000000	Piece	S
33>	593-L42AD01-01AP	INSERTION CARD ILO ENG LCT42HA36 USA P	1.000000	Piece	S
34>	60D-508015-00	MACH SCREW W/SPRING WASHER M5X0.8X15MM BLACK ZN PLATE	4.000000	Piece	S
35>	712-BP0402-01	STAND SUPPORT ASSY BP04 H=270MM BLACK	2.000000	SET	S
36>	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	1.000000	Piece	S
37>	E3421-925118	WIRE ASSY 8P2.5/7P2.0 L170MM 5V 12V SIGNAL POWER MT8202	1.000000	Piece	S
38>	E3421-925127	WIRE ASSY TJC3-2Y L860 SPK-R MT8202	1.000000	Piece	S

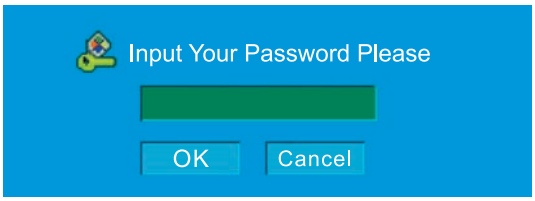
39>	E3421-925139	WIRE ASSY TJC3-3Y L760MM LCD37" MT8202 SPK-L	1.000000	Piece	S
40>	E3421-925153	WIRE ASSY 250MM 3WIRES 20# 1617 FOR POWER IN PUT	1.000000	Piece	S
41>	E3421-925195	WIRE ASSY LCT42" POWER BOARD TO MAIN BOARD 5V/5VSB/12V/24V L=300MM/330MM	1.000000	Piece	S
42>	E3461-000126	WIRE INVERTER 12P/2.0/10P/2.5 L350MM LCD42" (SUB INVERTER)	1.000000	Piece	S
43>	E3461-000127	WIRE INVERTER 12P/2.0/10P/2.5/3P/2.0 L700/500MM LCT42" INVERTER	1.000000	Piece	S
44>	E3471-000085	WIRE WS SHIELD WIRE LCT42" FOR MT8206 KEY	1.000000	Piece	S
45>	E3471-000090	WIRE WS SHIELD WIRE LCT422D L=300MM LPL MT8202 LVDS	1.000000	Piece	S
46>	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2.000000	Piece	S
47>	E6203-42PD02	DISPLAY LCD 42" LPL WXGA TFT LC420W02-SLA1	1.000000	Piece	S
48>	E7301-010002	BATTERY AAA R03P1.5V <2>	2.000000	Piece	S
49>	G244-34B811-01A	ROHS HANDLE FOR CARTON (DONGXU)	2.000000	Piece	S
50>	G300-L42AD01-02CA	ROHS POLYFOAM TOP L42AD (CHUANG YI)	1.000000	Piece	S
51>	G300-L42AD02-02CA	ROHS POLYFOAM BOTTOM L42AD	1.000000	Piece	S
52>	771BL27AD01-02	IR RECEIVE PCB ASS'Y FOR "ILO" LCD S-MT8202	1.000000	SET	S
53>	771KL422D01-01	KEY PCB ASS'Y FOR LCT422D S-MT8202	1.000000	SET	S

If you forget your V-Chip Password

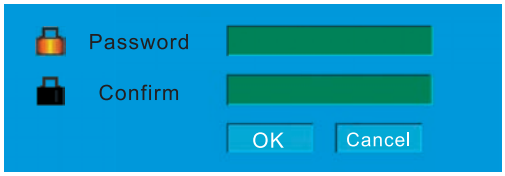
- Omnipotence V-Chip Password: 8202.

Using the “Change Password” item

1. When enter the “V-Chip” menu, select “Change Password”.
2. Press ▲ or ▼ button to highlight the “Change Password” item.
3. Press **Enter** button to confirm and pop up a menu.



4. Use 0~9 buttons input the omnipotence password(8202), then Press **Enter** button to enter and pop up a menu.



5. Use 0~9 buttons input your new password.
6. Press ▼ button to move to confirm blank.
7. Use 0~9 buttons input your new password again.
8. Press **Enter** button to confirm

-Suggest: Change to your familiar Password again.

Software Upgrade

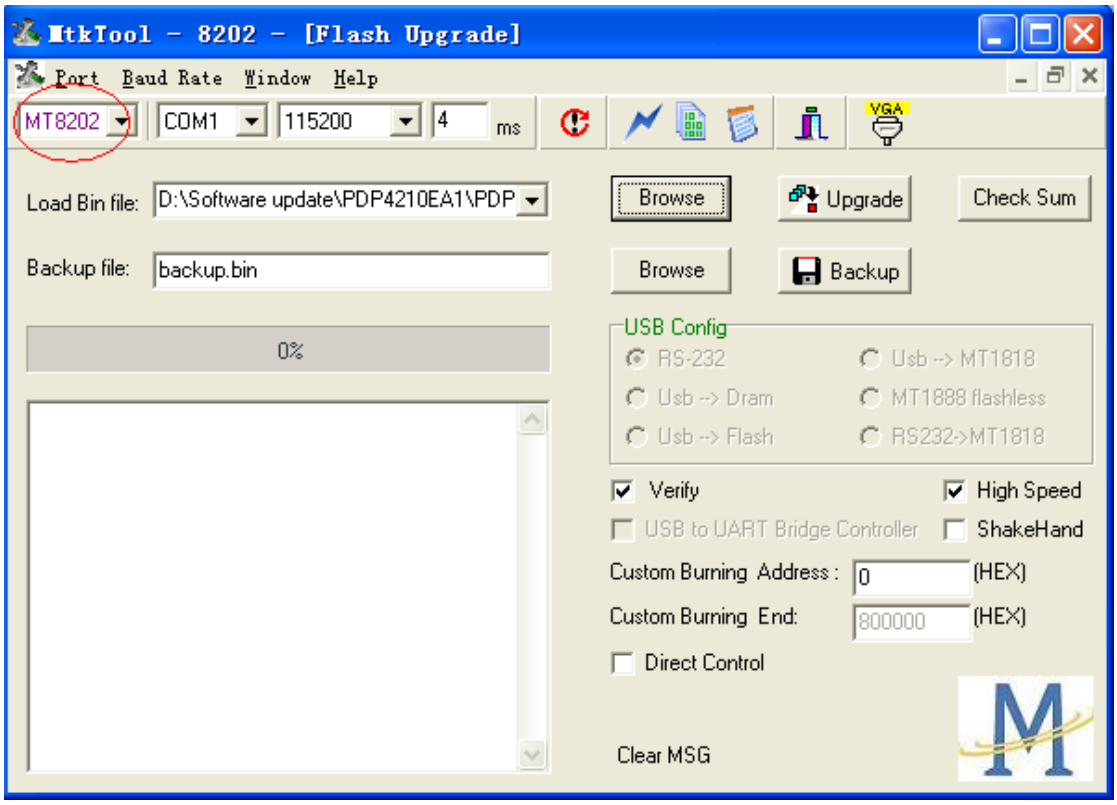
Process of update MT8202

Preparing :

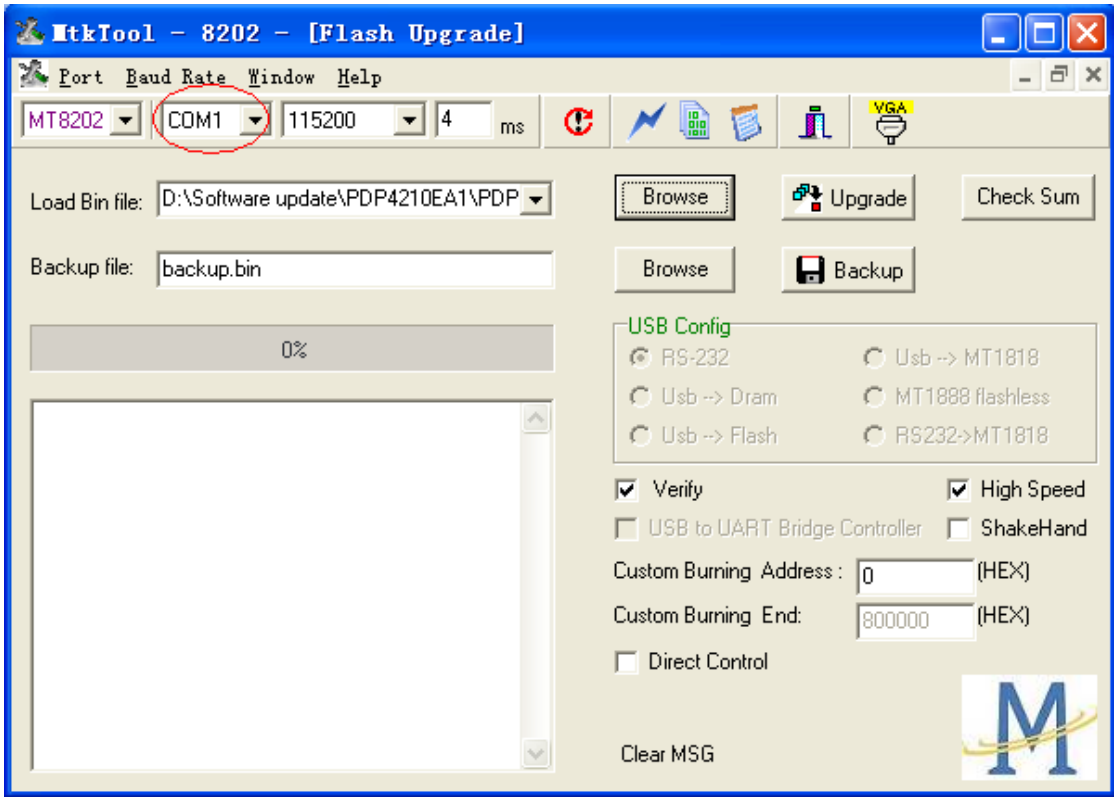
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC .

Downloading :

3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT8202. (the software of MTKtool will be sent to your side)

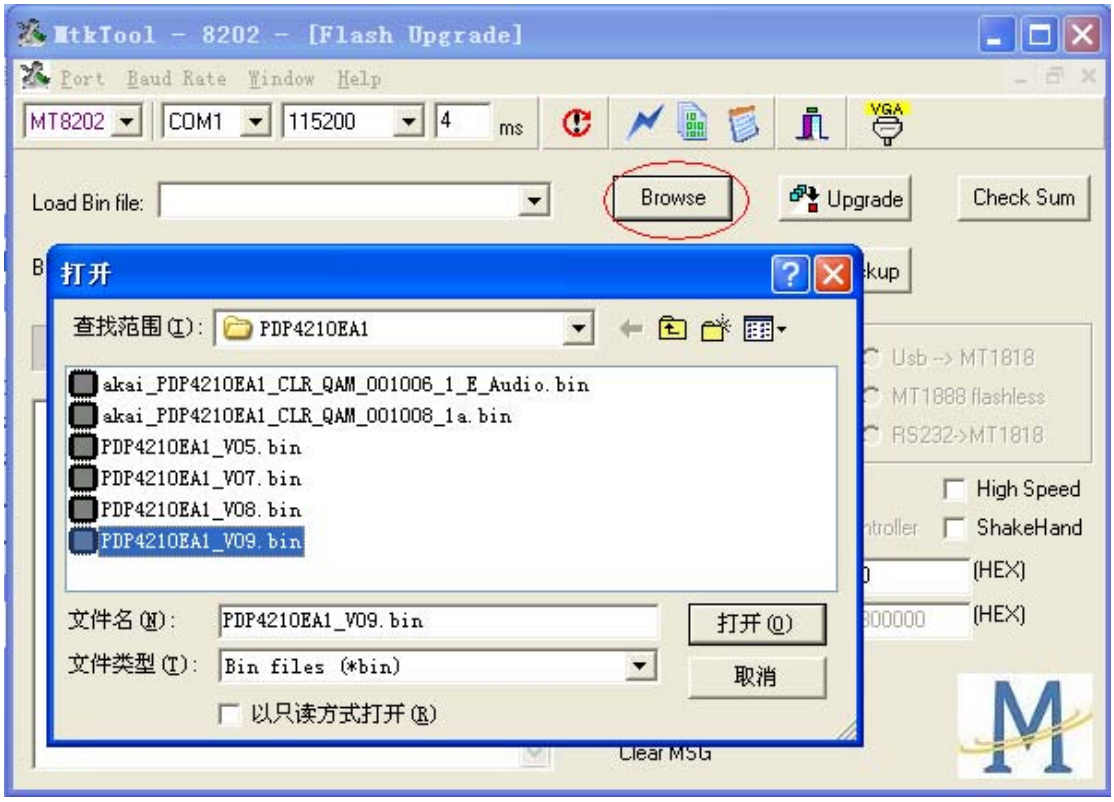


5. Select current COM port. (please try to check the COM port of your PC).

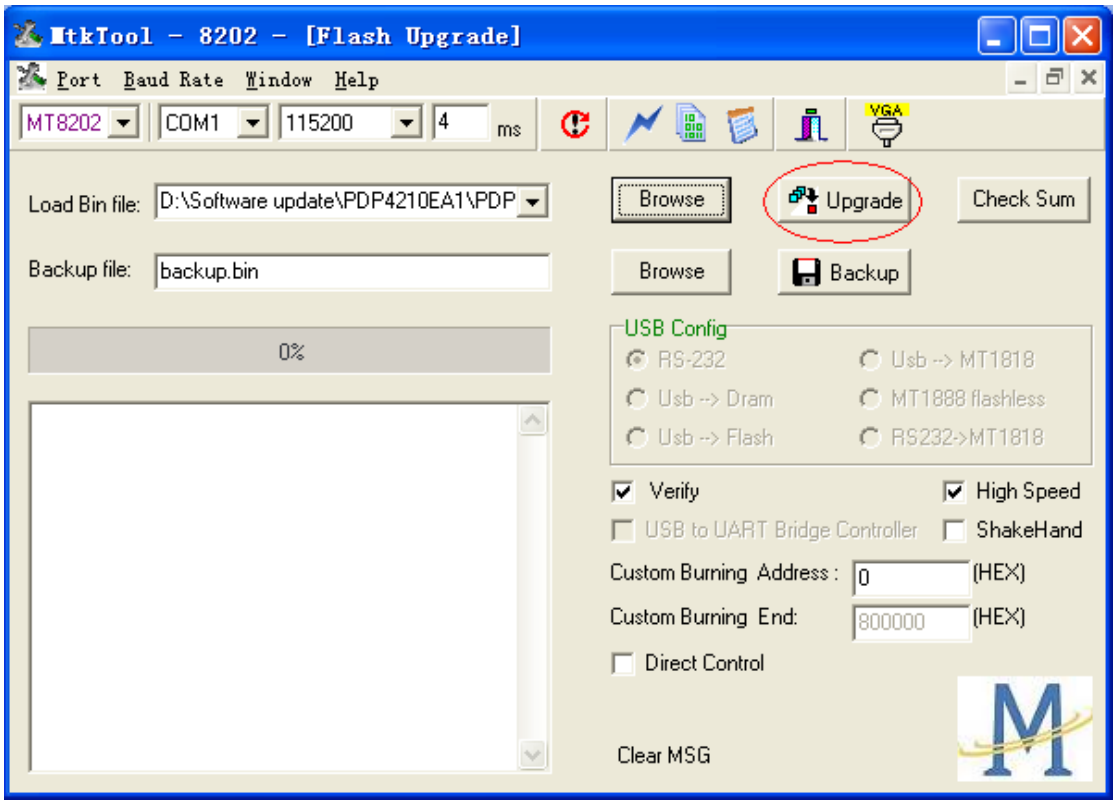


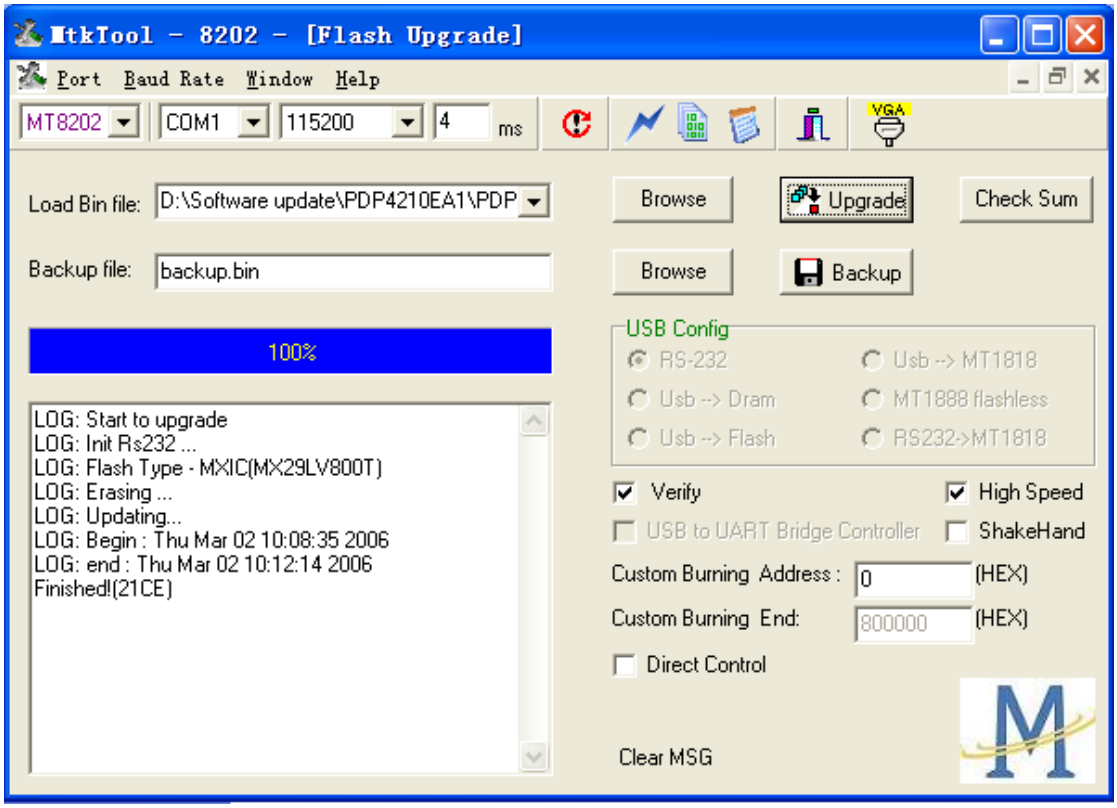
6. Choose the bit rate as 115200.

7. Select the update binary by pressing browse button. For example,the binary file name is PDP4210EA1_V09.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.





9. The update process is successful as the progress bar is 100%. After the update process is ok,

turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT8202 which has been download into the Plasma TV .

Press Menu button of the remote control，following input “8202”of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the mode of Firmware Version and then enter the mode of Firmware Version . It is easy to be found the version of the current firmware for MT8202 is as the following : “Factory ID : PDP4210EA1_VXX ”

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port

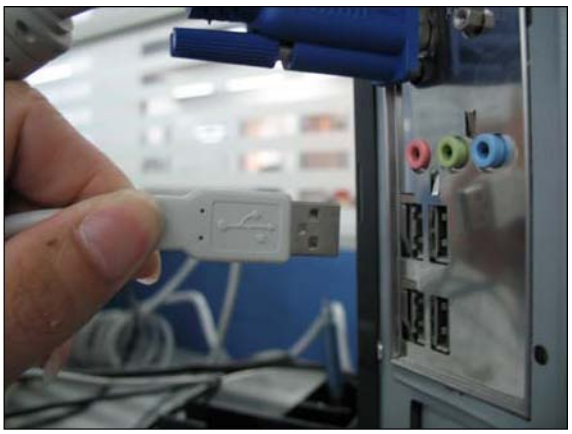
Connect another side of RS232 cable (#2) to the board (#1)

2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)

Connect RS232-VGA cable (#4) (VGA side) to the TV

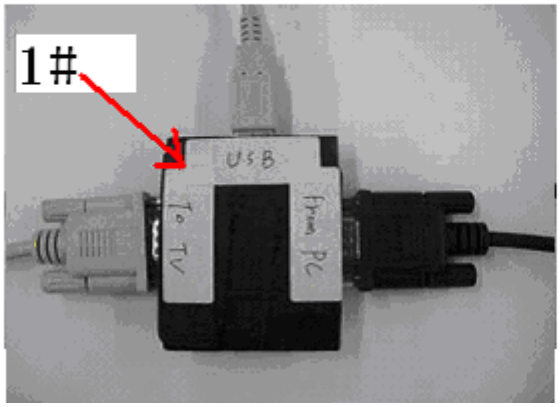
2.3 Connect USB cable (#5) to the board (#1)

Connect another side of USB cable (#5) to PC

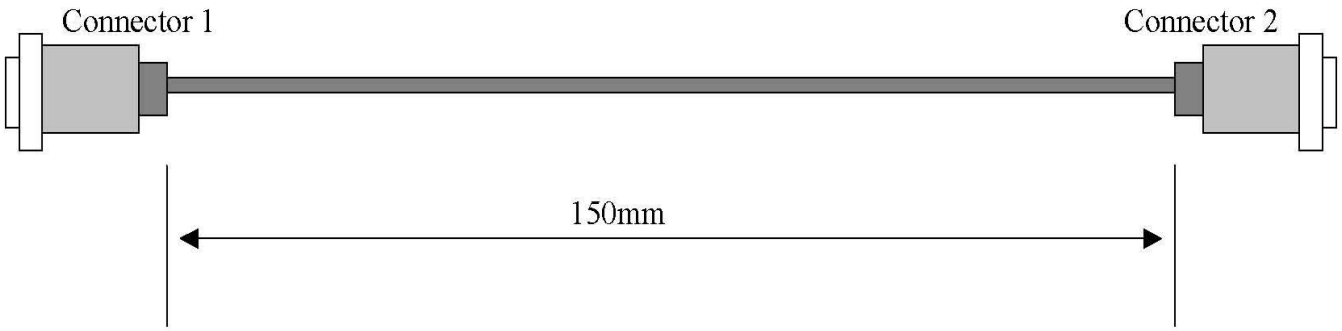


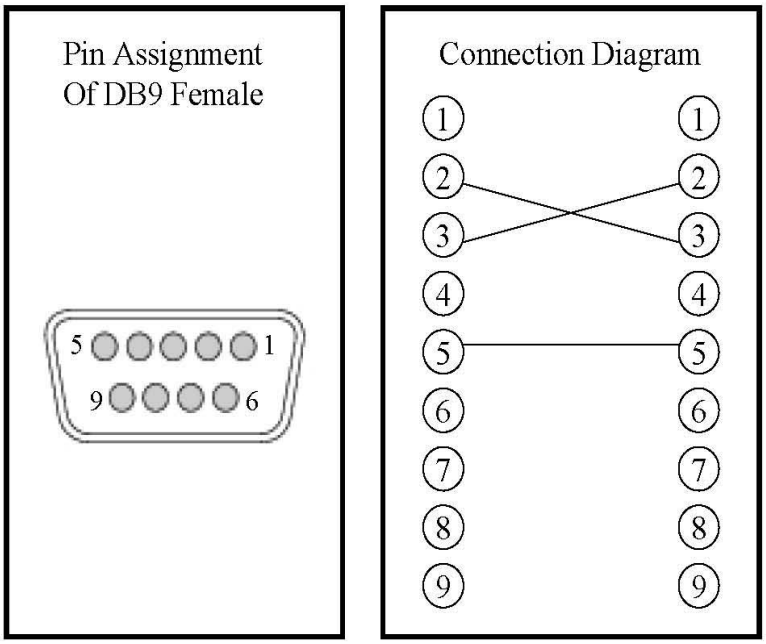
3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



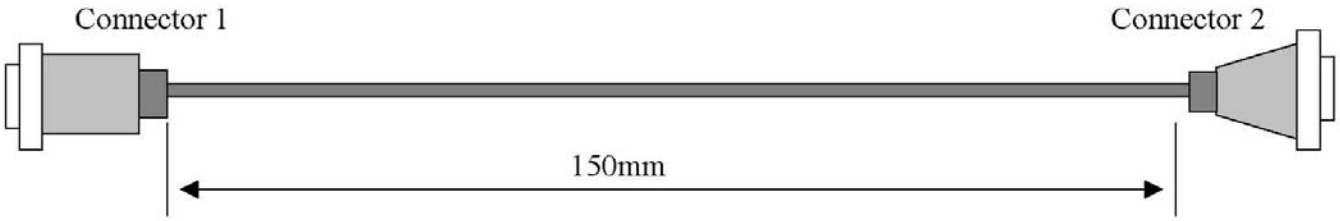
RS232 Null Cable for PC (#2)

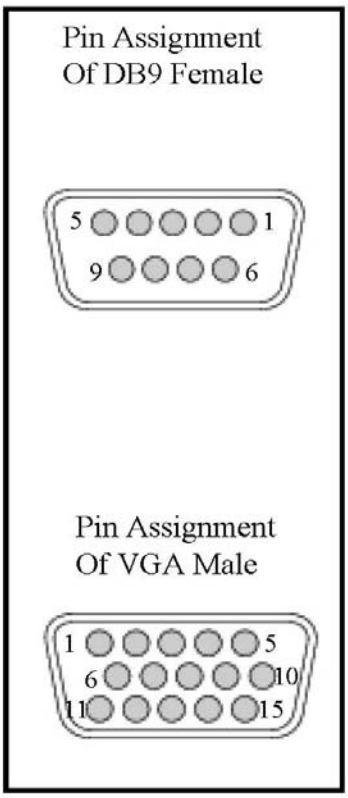


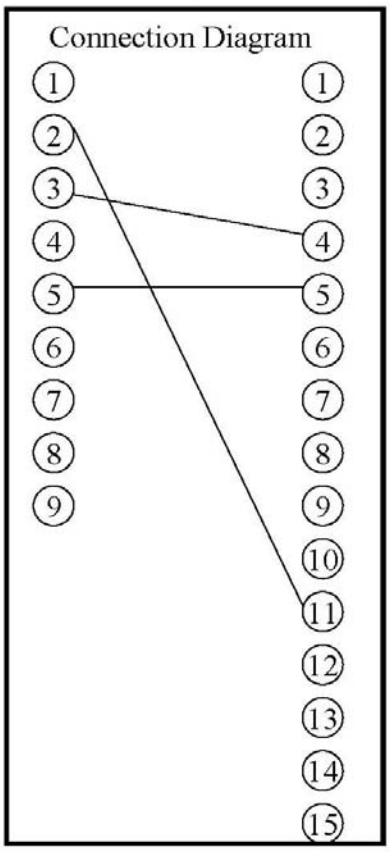


Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 - VGA Cable (#4)

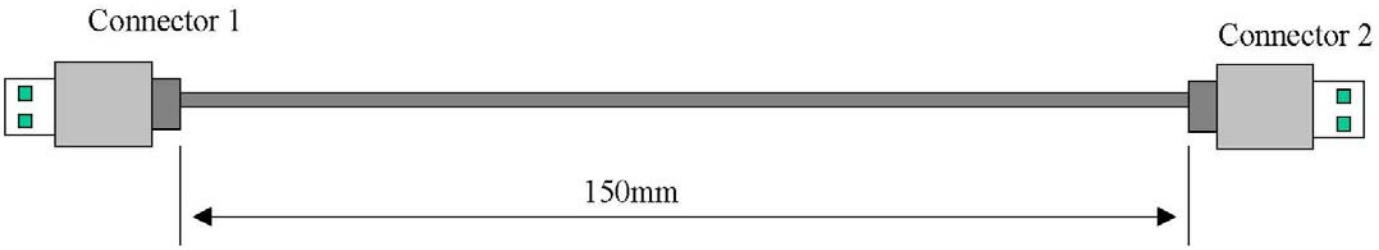






Connector 1: DB9 Female
Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male

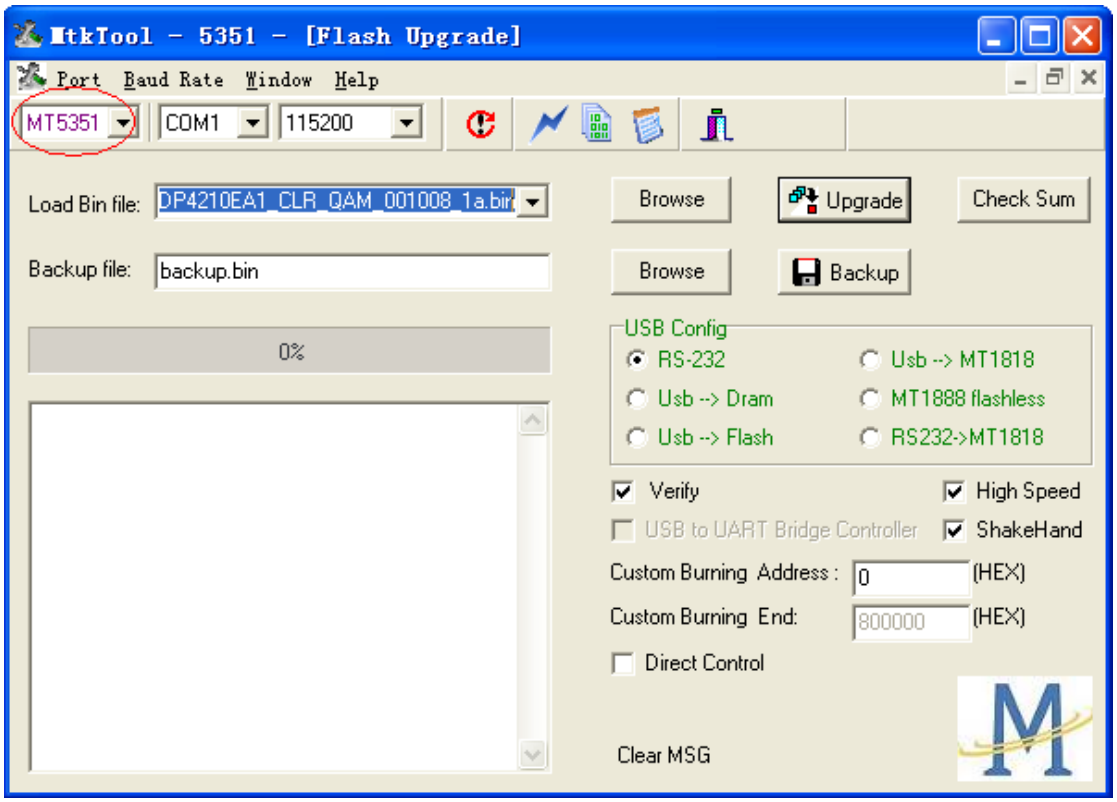
Process of update MT5351AG

Preparing :

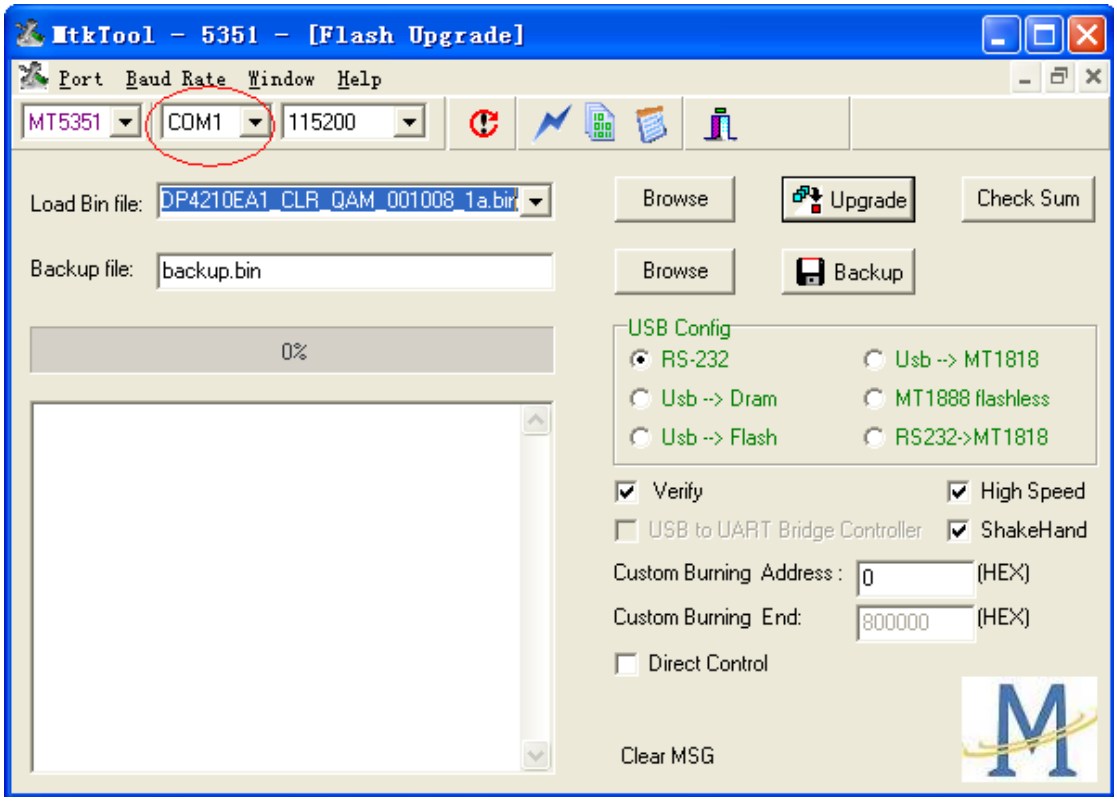
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC

Downloading :

3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT5351. (the software of MTKtool will be sent to your side)

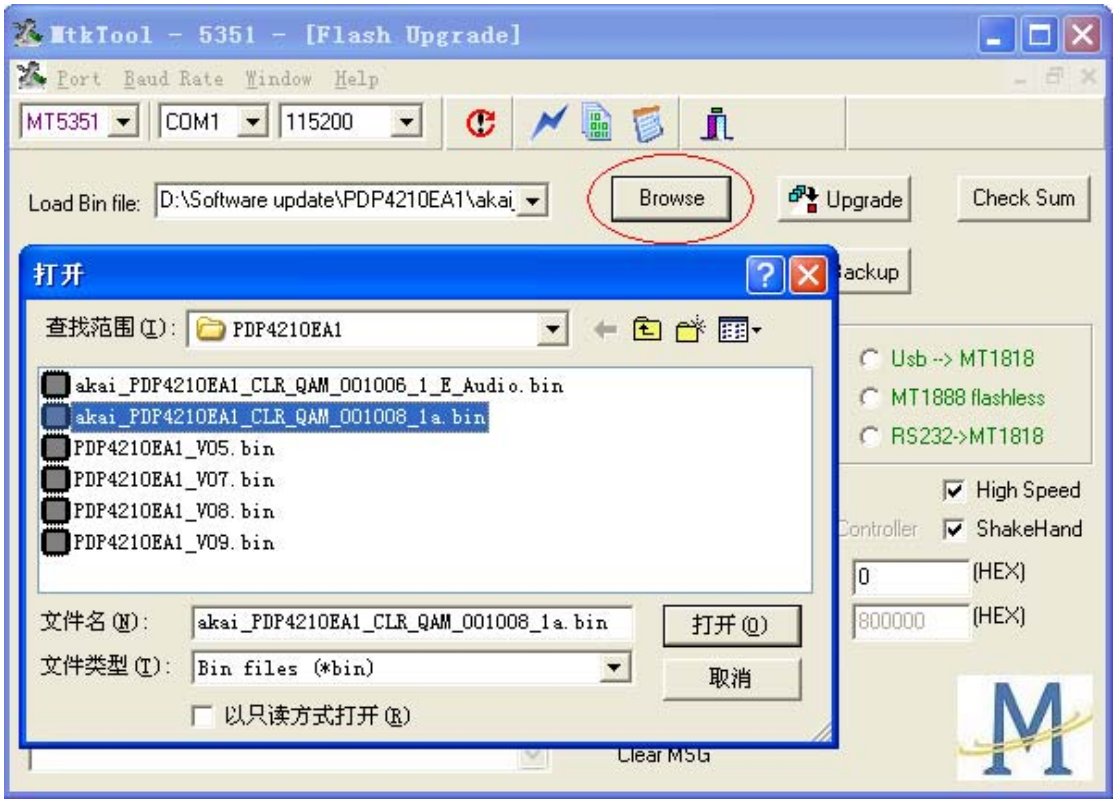


5. Select current COM port. (please try to check the COM port of your PC).

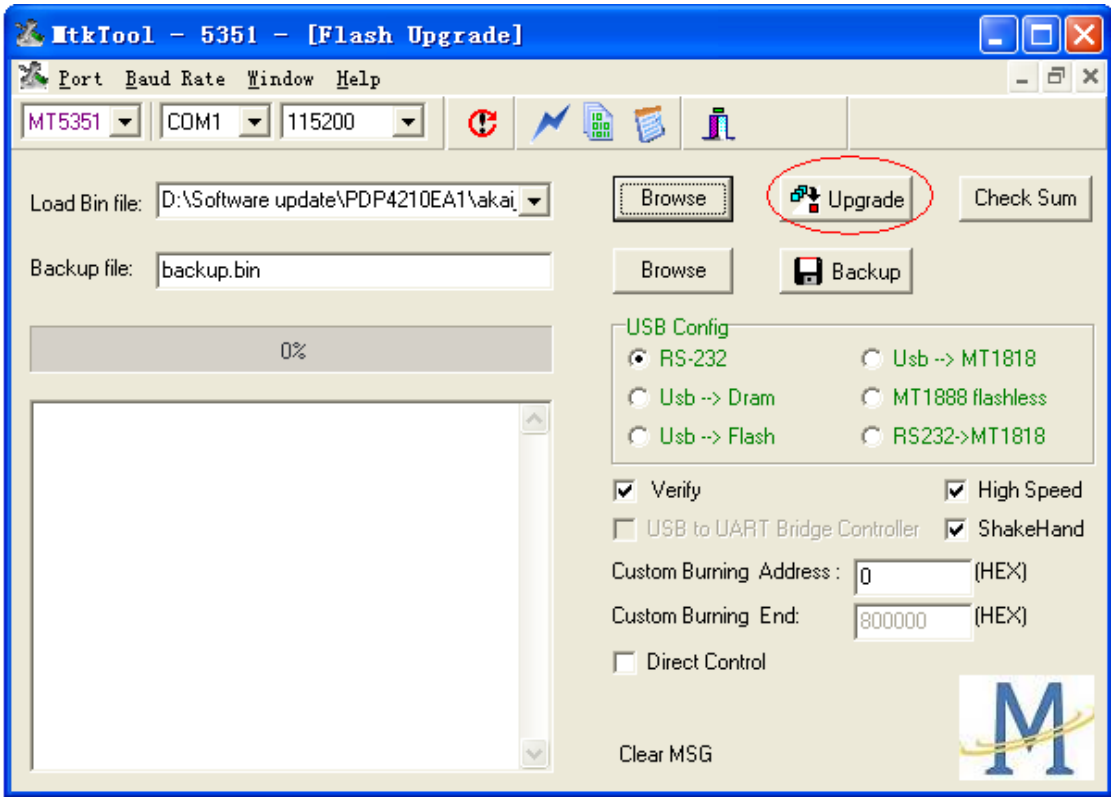


6. Choose the bit rate as 115200.

7. Select the update binary by pressing browse button. For example,the binary file name is XXXX_PDP4210EA1_000000XX_X_P.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking :

It is needed to check the version of the firmware for MT5351AG which has been download into the Plasma TV .

Press Menu button of the remote control and the main OSD menu is appeared on the screen .

Use the remote control and select the DTV menu . following input “0000” (zero , zero , zero , zero) of the remote control .Then enter the mode of factory after input the digits .

It is easy to be found the version of the current firmware for MT5351AG is “PDP4210EA1 CLA_QAM_XXXXXX_XX”under the mode of factory .

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 null cable x 1 for DTV (#3)
- USB cable x 1 (#5)

2. Installation for DTV upgrade

2.1 Connect RS232 cable (#2) to PC serial port

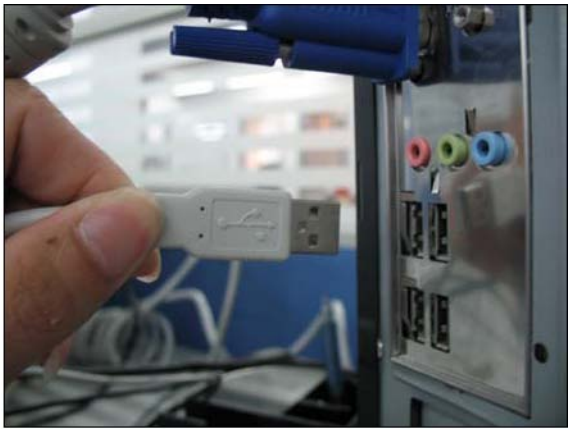
Connect another side of RS232 cable (#2) to the board (#1)

2.2 Connect RS232 cable for DTV (#3) to the board (#1)

Connect another side of RS232 cable for DTV (#3) to the TV

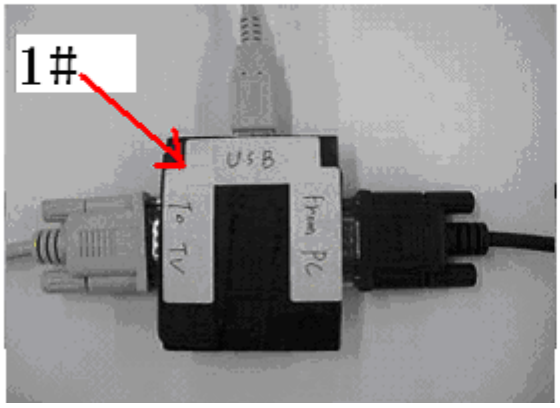
2.3 Connect USB cable (#5) to the board (#1)

Connect another side of USB cable (#5) to PC

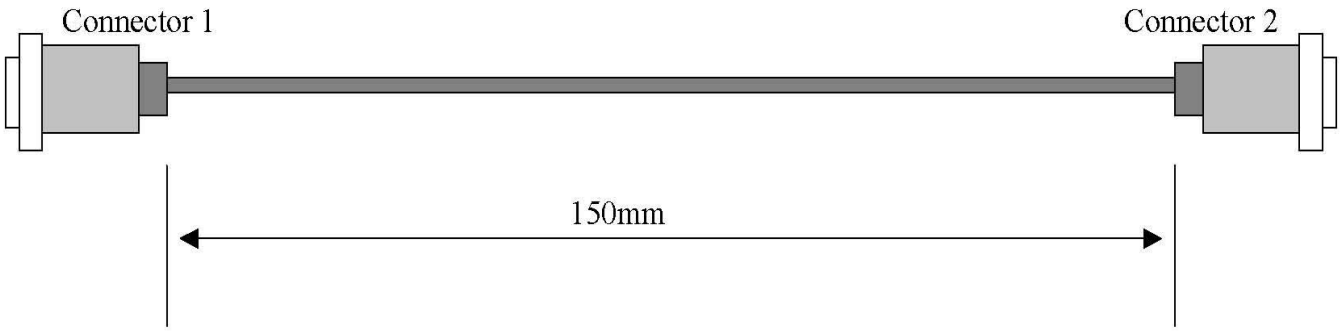


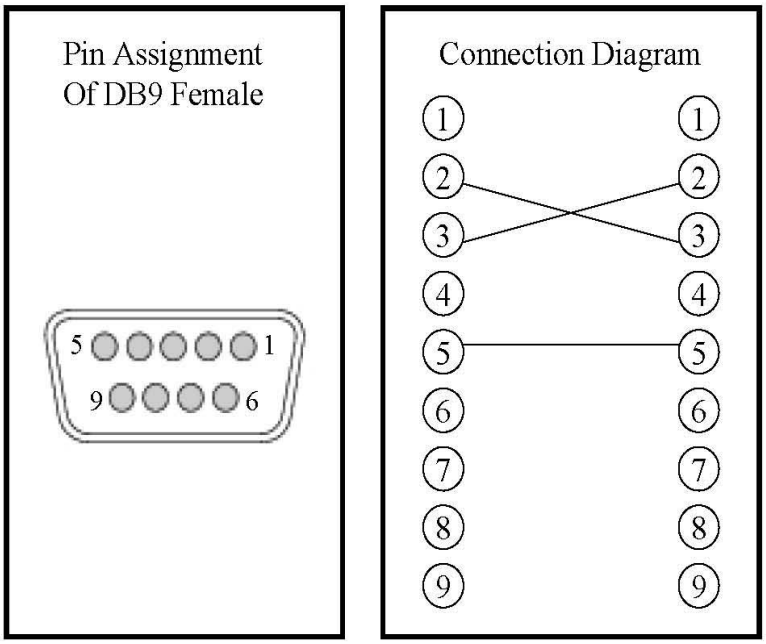
3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



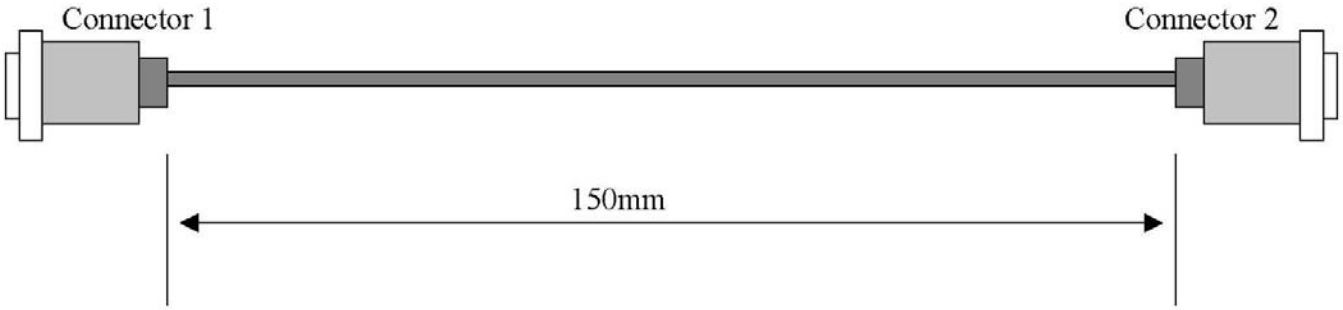
RS232 Null Cable for PC (#2)

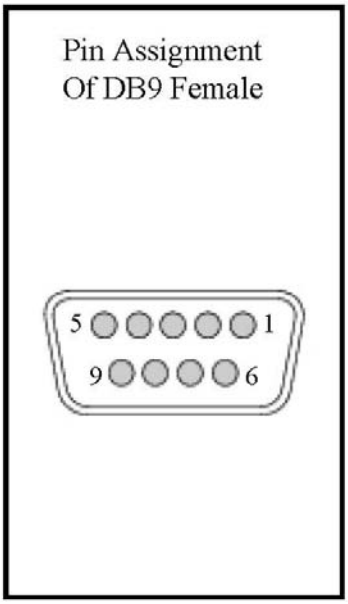


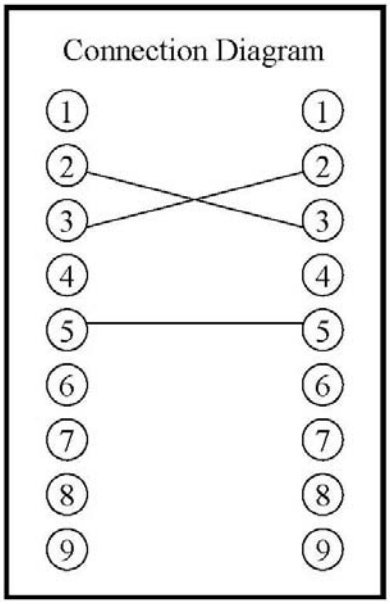


Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 Null Cable for DTV (#3)

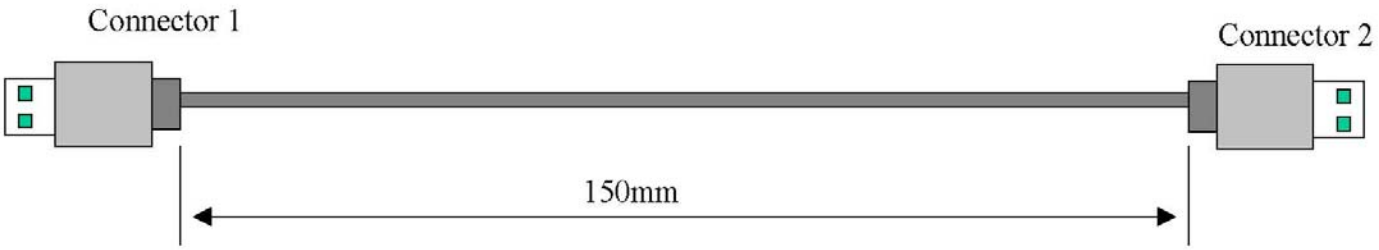






Connector 1: DB9 Female
Connector 2: DB9 Female

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male